Models
MX-354 & MX-356
Programmable Synchronous
Interface
Technical Manual

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REVISION HISTORY

ECO No.	Date	Description	Pages
0028	6/1/82	Per ECO	1-1
0046	8/23/82	Per ECO	6-1
0328	6/28/84	New ZETACO Cover	
0523	3/3/86	New Cover	

CUSTOMER SUPPORT HOTLINE

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PRODUCT RETURN AUTHORIZATION

All possible effort to test a suspected malfunctioning controller
should be made before returning the controller to ZETACO for repair.
However, if controller or module malfunction has been confirmed, you
should return the part to ZETACO. If the part is no longer under
warranty, or if the problem is not warranted, then repair will be on a
time-and-material basis. A Return Material Authorization (RMA) number
is required before shipment and should be referenced on all packaging
and correspondence.

To ensure prompt response, the information outlined in the Material
Return Information form on the following page should be gathered
before calling the ZETACO Hotline for the RMA number. Please include
a completed copy of the Material Return Information form with the
product. Each product to be returned requires a separate RMA number
and Material Return Information form.

To safeguard the product during shipment, please use packaging that is
adequate to protect it from damage. Mark the box "Delicate
Instrument" and indicate the RMA number(s) on the shipping label.

MATERIAL RETURN INFORMATION

All possible effort to test a suspected malfunctioning controller
should be made before returning the controller to ZETACO, Inc. for
repair. The speed and accuracy of a product's repair is often
dependent upon a complete understanding of the user's checkout test
results, problem characteristics, and the user system configuration.
Use the form below to record the results of your trouble-shooting
procedures. If more space is needed, use additional sheets.

TEST	RESULT
PSI DIAG	_____
UMUX REL I	_____
(or 4200)	

Other tests performed:

Please allow our service department to do the best job possible by
answering the following questions thoroughly and returning this
information with the malfunctioning board.

1. Does the problem appear to be intermittent or heat sensitive? (If
    yes, explain.)

2. Under what operating system are you running? (AOS, AOS/VS, RDOS,
    etc.)

3. Describe the system configuration (i.e.; peripherals, controllers,
    model of computer, etc.)

4. Has the unit been returned before?   Same problem?

To be filled out by CUSTOMER:

Model #: _____
Serial #:_____
RMA #:   _____(Call ZETACO to obtain an RMA number.)

Returned by:

Your name:_____
Firm: _____
Address: _____
           _____
Phone: _____

TABLE OF CONTENTS

MODELS MX-354, MX-356
PROGRAMMABLE SYNCHRONOUS INTERFACE (PSI/1-2)

1.0 INTRODUCTION

The Models MX-354 and MX-356 Programmable Synchronous Interfaces
are communications controllers designed to provide half or full duplex
synchronous communications control for a Data General Nova* or Eclipse*
based computer system.

The PSI/2 is a two-line controller and is fully compatible with the
programming formats of Data General's SLM-2 (4263) and MX-356 (4345)
synchronous line multiplexers.

The PSI/1 is a single line version of the PSI/2 and is compatible with
Data General's SLM-1 (4264) and MX-354 (4346)

Features of the controllers include: Programmable Line Characteristics
(word length, parity type, SNY Character, DLE Character), Full Modem
Control, 600-38.4K Baud Internal Clock and On-Board Cyclic Redundancy
Check (CRC).

The controllers may also be used in conjunction with a Data Control Unit
(DCU) to provide increased system performance. Each controller occupies
one slot in the CPU Chassis.

*Nova and Eclipse are registerd trademarks of Data General Corporation

2.0 INSTALLATION INSTRUCTIONS

2.1 UNPACKING

Upon receiving the interface package, unpack the contents and inspect
the board for visual damage. If any damage is apparent, do not attempt
to install the controller but notify ZETACO, Inc. immediately.

2.2 BOARD INSTALLATION

The controller board may be installed in any general I/O, memory - I/O
or I/O only slot of the Data General Nova or Eclipse mini-computer.
Install the controller in the desired slot, component side up and lock
into position with release levers (see Figure 2.1) CAUTION: Be sure
keyways in backplane connector line-up with slots in controller board
edge connector and arrows on ribbon cable plug match arrows on cable
connector (see Inset - Figure 2.1).
If with the selection of the I/O slot, a vacant slot or slots exist
between the controller and the board below it, the DCHP (Data Channel
Priority) and the INTP (Interrupt Priority) signals must be physically
jumpered on the computer backpanel to maintain priority interrupt
continuity. Install one end of a wire-wrap jumper to the DCHP - OUT
signal at pin 93 at the "A" connector occupied by the device below the
controller. Connect the remaining end to the DCHP - IN signal at pin 94
of the "A" connector occupied by the controller, bridging the vacant
slot or slots. Similarly, connect the INTP - OUT signal (pin A-95) from
the lower device to the INTP - IN signal at pin A-96 of the controller.
This will complete the priority interrupt continuity to the card. If
vacant slots exist between the controller and the device above the con-
troller, perform similar strapping of the DCHP and INTP signals to maintain
interrupt priority.
CAUTION: Be sure no existing cabling or devices are connected to the
          backplane of the slot the PSI is to be installed in.
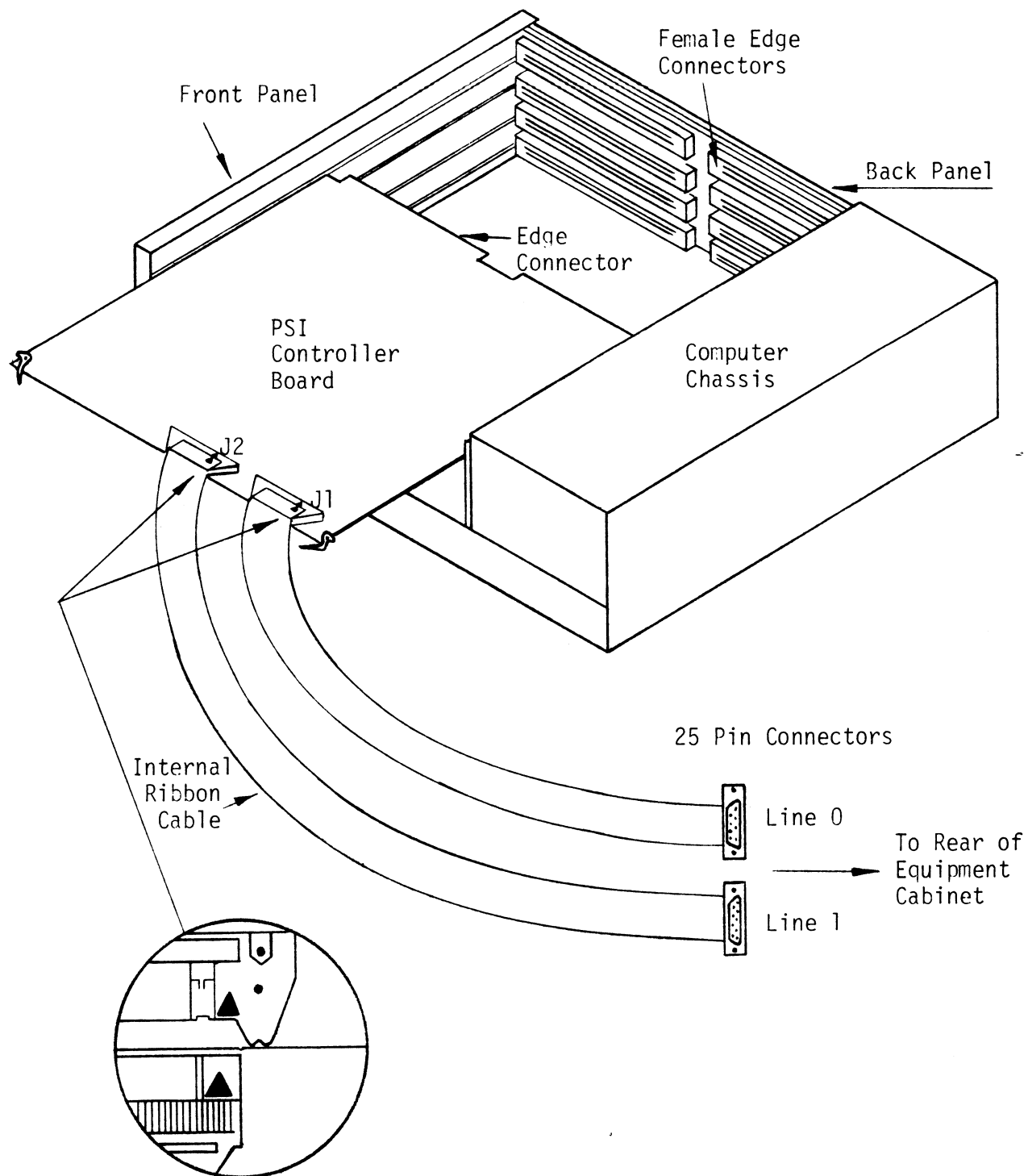
Front Panel

Female Edge
Connectors

Back Panel

Edge
Connector

PSI
Controller
Board

Computer
Chassis

J2

J1

Internal
Ribbon
Cable

25 Pin Connectors

Line 0

Line 1

To Rear of
Equipment
Cabinet

FIGURE 2.1 BOARD AND CABLE INSTALLATION

2.3 CABLES (refer to Figure 2.1)

Ribbon cables provide communication interfacing for the PSI. The
cable plugs into the 26-pin header located on the front edge of the
controller board.

NOTE: When plugging the connector in, be sure to line up the arrows
on the connector and header to assure proper connection.

On PSI/2 boards, separate cables are used for each line. As viewed
from the front edge of the board, the right-most header is used for line 0
and the left header for line 1.

The ribbon cables should then be pulled through to the back of the
computer equipment cabinet. An external cable may then be connected
to the 25S connector of the ribbon cable and secured using the
jack screws. For PSI/2 boards, be sure the external cables are connected
to the proper ribbon connectors, line 0 or line 1.

When installation is complete, the ribbon cables should be secured to
the computer chassis.

2.4 COMPUTER BACKPANEL

The backpanel of the computer provides a means for interconnecting the
computer, memory, console and various controller boards and cabling to
external peripheral equipment. The back panel is the vertical printed
circuit board mounted on the left side of the computer chassis when
viewed from the front.

On the side of the back panel facing into the chassis are pairs of
printed circuit board female edge connectors, one pair for each slot.
The contacts of these connectors protrude through the back panel to the
left side of the minicomputer chassis.

When the male edge connectors of a printed circuit board are inserted
into the female edge connectors of a slot, finger contacts on the male
edge connectors meet contacts in the female edge connectors. Electrical
connections to boards can, therefore, be made to pins on the back panel.

For each controller card slot, there are two horizontal parallel rows
of 100 pins on the backpanel. The left group of pins is the A connector,
and the right group (as viewed from the left side of the computer) is
called the B connector. Numbering of each group of 100 pins is as
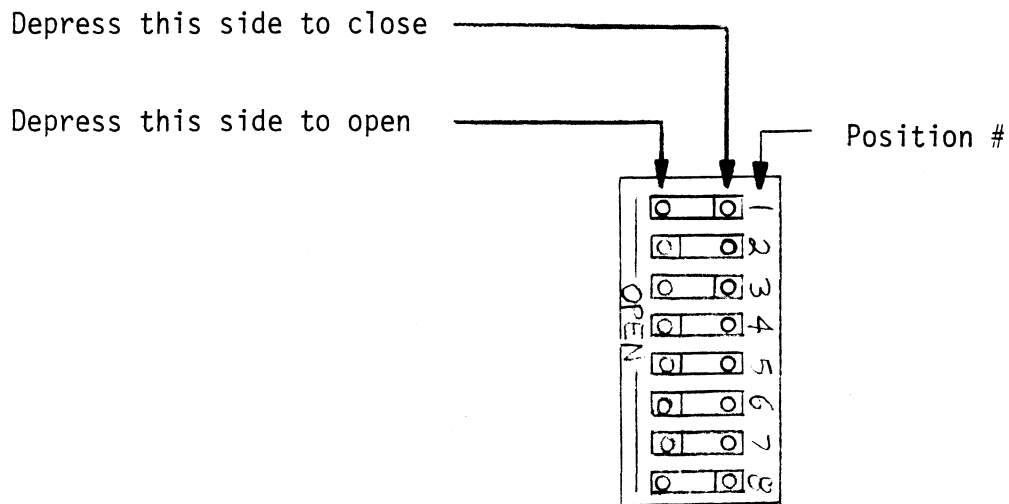indicated below (shown only for connector A).

BACK PANEL NUMBERING

A1	A3	A5	A7	A9	A11	A13	A15	A17	A19	A21	A23	A25	A27	A29	A31	A33	A35	A37	A39	A41	A43	A45	A47	A49	A51	A53	A55	A57	A59	A61	A63	A65	A67	A69	A71	A73	A75	A77	A79	A81	A83	A85	A87	A89	A91	A93	A95	A97	A99
A2	A4	A6	A8	A10	A12	A14	A16	A18	A20	A22	A24	A26	A28	A30	A32	A34	A36	A38	A40	A42	A44	A46	A48	A50	A52	A54	A56	A58	A60	A62	A64	A66	A68	A70	A72	A74	A76	A78	A80	A82	A84	A86	A88	A90	A92	A94	A96	A98	A100

3.0 CONFIGURATION

Processor selection (CPU/DCU), device codes, line address, local
clock speed, and +12 Volt power source are selectable and should be
checked and configured per system requirements before installation.
To do this, the board cover must be removed.

Switch functions are indicated near the switches. Each switch consists
of eight individual switches numbered 1-8 (see below). Jumpers are
also used and are "IN" if the foil is not cut or a wire is in its place.
Jumpers are "OUT" if the foil is cut or wire removed. Use 24 gauge
solid insulated wire for jumper replacement.

Depress this side to close ─────────────────┐
                                            │
Depress this side to open ────────────┐   │
   │   │   ┌─── Position #

Switch is shown with positions 1, 3 and 8 closed; all other
positions are open.

3.1 PROCESSOR (CPU/DCU) SELECTION

The PSI/1-2 may be configured to operate in one of two modes-the
first is the CPU mode-in this mode, the controller board responds to
commands from the CPU via the backplane. This requires the CPU to
handle all communications on a character to character basis-greatly
increasing processor overhead.

The second mode, or DCU mode allows a Data Control Unit to directly
control the PSI. The PSI resides in the CPU chassis using only power
from the backpanel. A jumper plug is used to pass signals from the
DCU/50 or DCU/200 to the controller board. One or more PSIs may be
daisy-chained off the DCU to provide several synchronous lines with
minimal system overhead.

Units from the factory are initially set up to operate in the CPU
mode. To operate using the DCU, jumper J2-3 (located near chip loc. B4)
must be cut or out, and two jumper plugs must be installed on the
backplane. (see below)

PSI SLOT

DCU SLOT

BACKPLANE

50/60Hz JUMPER

CPU
CHASSIS
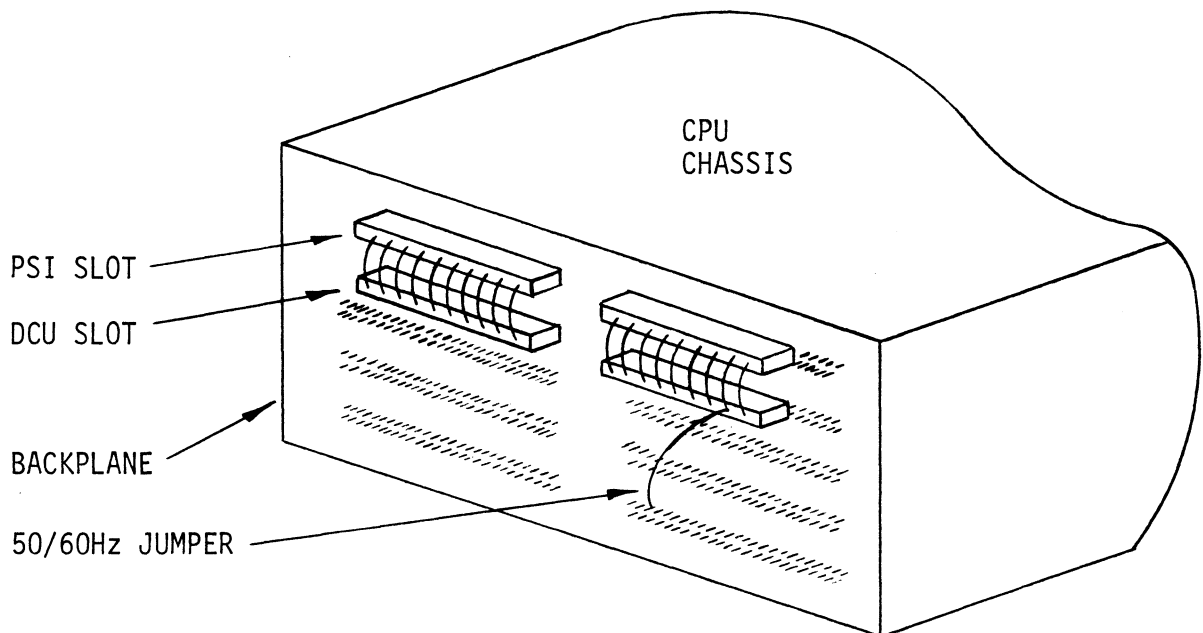
3.2 DEVICE CODE SELECTION

The line sections and the CRC sections of the PSI board are accessed
via two separate device codes. Mnemonics are MUX and CRC. The MUX
is always an even device code and CRC is always the next higher
consecutive odd device code. Primary device codes for MUX and CRC
are 34_8 and 35_8, respectively, and secondary device codes are 44_8,
45_8. The device code select switch, however, allows the user to select
any pair of consecutive device codes. Refer to the figure below to set
the desired device code.

NOTE: The switches must be set to the MUX (even) device code.

DEVICE CODE SELECT SWITCH (location X-2)
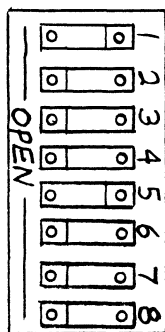
|	
SW1 = DS0	
SW2 = DS1	Open = Logic "1"
SW3 = DS2	Closed = Logic "0"
SW4 = DS3	
SW5 = DS4	
SW6 = Not Used	
SW7 = Not Used	
SW8 = Not Used	

SHOWN:
Device codes 34_8 (MUX) and 35_8 (CRC) selected.

3.3   LINE ADDRESS SELECTION

The methods for selecting and setting the line address of the PSI vary depending on the board type.

- For single line boards (PSI/1), any line address in the range 0-377_8 may be selected.

- For dual line boards (PSI/2), any two consecutive line addresses in the range 0-377_8 may be selected, with line 0 representing the lower, even line number, and line 1 representing the higher, odd line number. The switch must be set to the lower (even) address. (See below)

LINE ADDRESS SWITCH (Location W-4)
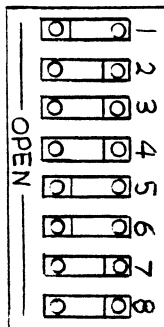

```
SW1 = Line Sel 0 (least significant)
SW2 = Line Sel 1
SW3 = Line Sel 2        Open   = Logic "1"
SW4 = Line Sel 3        Closed = Logic "0"
SW5 = Line Sel 4
SW6 = Line Sel 5
SW7 = Line Sel 6
SW8 = Line Sel 7 (most significant)
```

NOTE 1: SW1 (Line Sel 0) is only used on single line boards. (PSI/1)

NOTE 2: On PSI/2 boards, line address must be set to lower (even) line number.

SHOWN: Line 61_8
         Selected

3.4 LOCAL CLOCK SPEED SELECTION

Timing for transmitting and receiving synchronous information is usually provided to the PSI by the modem unit. However, an on-board local clock is provided on the PSI board and may be used for timing if externally clocked modems are used, or if a data link is made without modems. Baud rates are available from 600 to 38.4K baud, and are selectable using the Local Clock switch. (see below) Local clock signals are not connected internally. They must be looped back; this is usually done through the modem, but may require special cabling considerations for direct data links. (see Section 6.1.2)

LOCAL CLOCK SWITCH (location C-9)
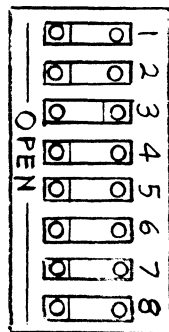

```
SW1 = 38.4K Baud
SW2 = 19.2K Baud
SW3 =  9.6K Baud
SW4 =  4.8K Baud
SW5 =  2.4K Baud
SW6 =  1.2K Baud
SW7 = 600    Baud
SW8 = Not Used
```

NOTE: Close switch to select rate; only one switch may be closed at a time.

SHOWN:
9.6K Baud

3.5 +12 VOLT POWER SOURCE

The PSI requires +12 Volts for proper operation of the RS-232C driver
chips. The source of the +12V depends on the machine being used. On
older machines (Nova 1200, 2, 3 etc.),the +12V is regulated down from
+15V (VINH - pin A10). In a newer machine (Nova 4, Eclipse S140),
+12V is available on backplane pin B90. Jumpers J2-1 and J2-2 (located
near chip loc A10) are used to select between the two sources.

- The PSI is factory set for +15V to +12V regulation, as used with
  a Nova 1200, 2, 3, etc. J2-2 is IN and J2-1 is OUT, or cut.

- To change the configuration for use with a +12V source, cut or
  remove jumper J2-2, and insert a 24 gauge wire into jumper J2-1.

4.0 OPERATION

Each line of the Programmable Synchronous Interface consists of Receiver,
Transmitter, and Modem Control sections. All sections of both lines use
the same device code, and each section may set the Done Flag if it is
enabled and requires service.

If more than one section is requesting service at the same time, the
section of highest priority will be serviced first. For each line, the
receiver section has higher priority than the transmitter section, which
in turn has higher priority than the modem control section. Also, for
PSI/2 boards, each section of the lower number line has higher priority
than the corresponding section of the higher number line. (see below)

```
Line 0        Receiver      -  Highest Priority
Line 1        Receiver      -
Line 0        Transmitter   -
Line 1        Transmitter   -
Line 0        Modem Control -
Line 1        Modem Control -  Lowest Priority
```

Also on the PSI controller is the CRC generator/checker, used by the
receiver and transmitter sections of both lines. The CRC section uses the
next higher device code than that of the other sections. The Busy Flag is
active while the CRC is performing a calculation.

The PSI operates in two modes, Offline (diagnostic) and Online (normal).
In Offline mode the program provides timing pulses for onboard counters
and sequenced logic via I/O Pulse commands. In normal mode, timing is
provided by the on-board oscillator.

4.1 DONE, BUSY AND DEVICE FLAG COMMANDS

Mnemonics for PSI programming are MUX and CRC, with MUX commands controlling receiver, transmitter, and modem control sections, and CRC commands controlling the CRC section. Start and Clear commands are meaningless unless the board is enabled. This may be done with a Set Line and Section (DOA) instruction.

Done, Busy and Device Flag commands for the MUX sections are:

Busy Flag	-	Not used
Done Flag	-	Active whenever an enabled line section of the board requires service.
F=S	-	Start pulse - clears all done flags on board, puts all sections of board offline except local clock and CRC timing clock (if online), and initializes board logic.
F=C	-	Clear pulse - clears done Flags of board and current line section, and puts all sections of board online.
F=P	-	I/O pulse - steps internal control clock if in offline mode; has no effect in online mode.

Done, Busy and Device Flag commands for the CRC section are:

Busy Flag	-	Active while CRC is performing a calculation.
Done Flag	-	Not used
F=S	-	Start pulse - starts CRC calculation
F=C	-	Clear pulse - clears CRC logic and partial result register.
F=P	-	I/O pulse - steps local clock and CRC timing clock if in offline mode; has no effect in online mode.

4.1 DONE, BUSY AND DEVICE FLAG COMMANDS (cont.)

I/O Reset   - Same as start command to MUX, however goes to all
                        boards in chassis. (same as power on). Also puts
                        local clock and CRC timing clock in offline mode.

4.2 INITIALIZATION AND SETUP

The PSI is initialized by an I/O Reset instruction. A start MUX command
may be used if the board is first enabled with a Set Line and Section
(DOA) instruction. Logic is initialized, Done Flags cleared, and the
board is placed in offline mode. All receiver and transmitter sections
will be turned off, modem control sections will be turned on, and
transmitters will be set for non-transparent operation. Modem control
output signals and line characteristics are not affected.

The Set Line and Section (DOA) instruction may then be used to select
which line and section are current, or to which succeeding instructions
will pertain to. This line/section remains current until set with
another Set Line and Section instruction or a Read Line and Section
Requesting Service (DIA) instruction.

The board may then be set up for operation by configuring each line
with operating characteristics, each receiver with a SYN character, and
each transmitter with SYN and DLE characters. Line characteristics must
be specified prior to setting SYN and DLE characters to insure that proper
parity is appended. The board is then placed online with a Clear MUX
command, and the necessary line sections turned on with Control Line
Section (DOC) instructions. The Modem Control and CRC sections may also
require set up before operation is to begin.

4.3 RECEIVER

The receiver section of a line receives the synchronous data serially
from the modem and assembles the data into characters which are then
received (with parity) by the processor over the data bus. Following
initialization and setup, the receiver is turned on with a Control Line
Section (DOC) instruction. It then monitors the serial bit stream
until it receives at least two successive SYN characters. It will then
assemble the next non-SYN character and set Done. A Read Line and
Section Requesting Service (DIA) instruction is executed to determine
which line and section requested service. A Read Received Data (DIB)
instruction will pass the character, right-justified onto the processor
data bus. Parity is retained for CRC calculations.

Receiver errors (parity, overrun) may then be checked with a Read
Receiver Status (DIC) instruction. This data, however, will only be
valid if read after received data has been read from the receiver. If
it is discovered that a modem section has requested service rather than
the receiver, this data represents new modem status, and the data read
from the receiver becomes invalid. After verification of receiver status,
the program may issue a Start command to the CRC to calculate a new CRC
word.

The program may change line characteristics (with the exception of word
length) while the receiver is turned on.

4.4 TRANSMITTER

The transmitter section of a line handles the serialization of data to
be passed to the modem. Following initialization and setup, the transmitter
is turned on with a Control Line Section (DOC) instruction, after which

4.4 TRANSMITTER (cont.)

it will immediately set Done, indicating that it is ready to accept
a character for transmission, and begin to underrun. The underrun consists
of a series of SYN characters transmitted if the transmitter is in non-
transparent mode or DLE character - SYN character pairs if transmission is
in transparent mode.

Data may be transmitted via Transmit Data (DOB) instruction. When the
transmitter is ready to accept another character, Done will set. A Data
In-A is executed to determine which line/section requested service. The
Done condition may be cleared by a NIOC or DOBC MUX instruction.

Bits 2 and 3 of the transmit data accumulator control the transmission mode,
either non-transparent or transparent. If the mode of operation is
changed, the transmitter will insert a DLE character before the transmitted
data.

An inactive Clear to Send signal from the modem will cause transmission to
cease and the output will be held in the mark state. When CTS becomes
active transmission may resume. A Transmit Underrun Sequence (DOB)
instruction causes the transmitter to underrun and inhibits Done from
setting until another Transmit Data instruction.

4.5 MODEM CONTROL

If the board is online, the modem control section will set Done when any
of the four status signals (Carrier Detect, Clear to Send, Data Set Ready
and Ring Indicator) from the modem change state. The new status may be
read and Done cleared with a Read Modem Status-clear (DIC-C) instruction.

4.5   MODEM CONTROL (cont.)

Modem control output signals are set up or changed with a Set Modem
Control Status (DOB) instruction. Programming of the modem control
section may vary depending on the modem used. The modem user's manual
should provide information on the functions of the control signals.

4.6   CRC

The CRC (cyclic redundancy check) generator/checker section is used
to calculate a 16-bit word which assists in the detection of errors
when a block of data is transferred over the synchronous line. The
CRC section is placed on-line along with the rest of the board with
a Clear MUX command, however, it can only be placed offline with an
I/O Reset instruction. Once on-line, it must be cleared with a Clear
CRC command before being used.

Whenever processor data is read from a receiver or sent to a transmitter,
it is sent to the CRC section. A start CRC command will then cause a new
CRC word to be calculated. Because the CRC section is used by each
receiver and transmitter section it may be necessary to use the Read
CRC Partial Result (DIB) and Load CRC Partial Result (DOB) instructions
each time a different section is service, in order to maintain calculations.
When re-loading a partial result, the CRC section must first be cleared
with an NIOC or DIBC command.

4.7 LOOPBACK

Either line may be placed in loopback mode with a Specify Line
Characteristics (DOC) instruction. Loopback mode provides for the
testing of each line by connecting the transmitted data path to the
received data input. The local clock is used for all timing and Clear
to Send is forced active.

For normal operation, loopback mode must be off.

5.0   PROGRAMMING NOTES

The PSI/1-2 controller responds to fourteen instructions which control
the various functions of synchronous communications. Some instructions
are used more than once, with AC Bits 0, 1 and 15 determining the specific
function. All instructions apply only to the current line address once
it has been established with a Data Out-A or Data In-A. Mask bit for
MUX is 8. The instructions are as follows:

1)   Set Line and Section
     DOA (f) AC, MUX

```
┌──────────────────┬──────────────────────┬────┐
│ 0              6 │ 7                  14 │ 15 │
└──────────────────┴──────────────────────┴────┘
```

Section:

    0=Receiver
    1=Transmitter
    0 or 1=
      Modem Control

Line Address:
    0-377$_8$

Not Used
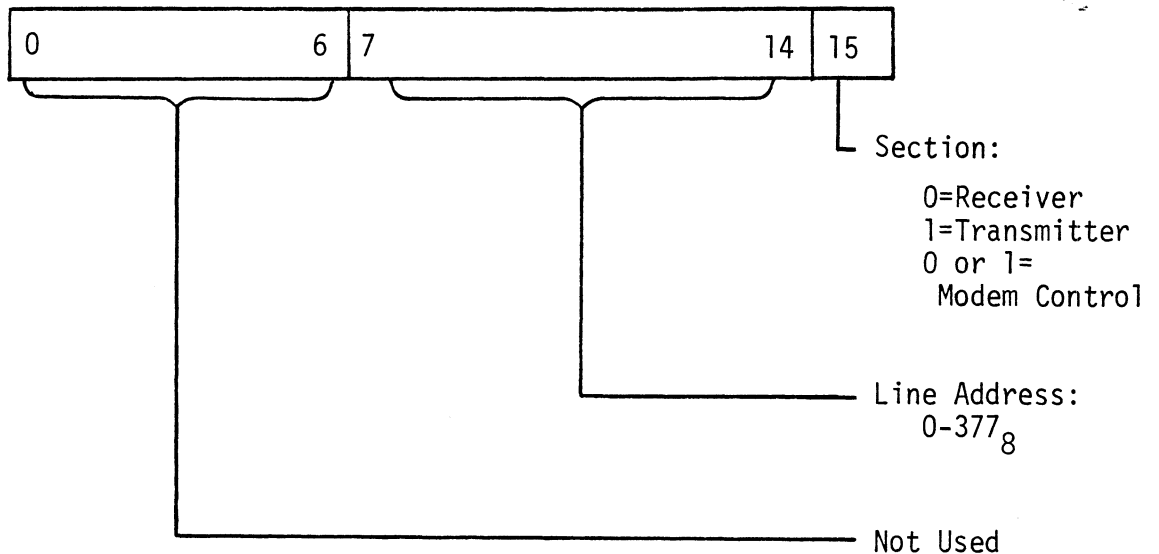
5.0 PROGRAMMING NOTES (cont.)

2) Transmit Data
    DOB (f) AC, MUX

```
┌─────┬─────┬─────────┬───────────────┐
│ Ø  1│ 2  3│ 4     7 │ 8          15  │
└─────┴─────┴─────────┴───────────────┘
```

Character to be transmitted
right justified with unused
and parity bits=Ø

Not used

Transmission Mode:

   ØØ No Change
   Ø1 Not Used
   1Ø Insert DLE and leave
       transparent mode
   11 Insert DLE and enter
       transparent mode

Must be = ØØ
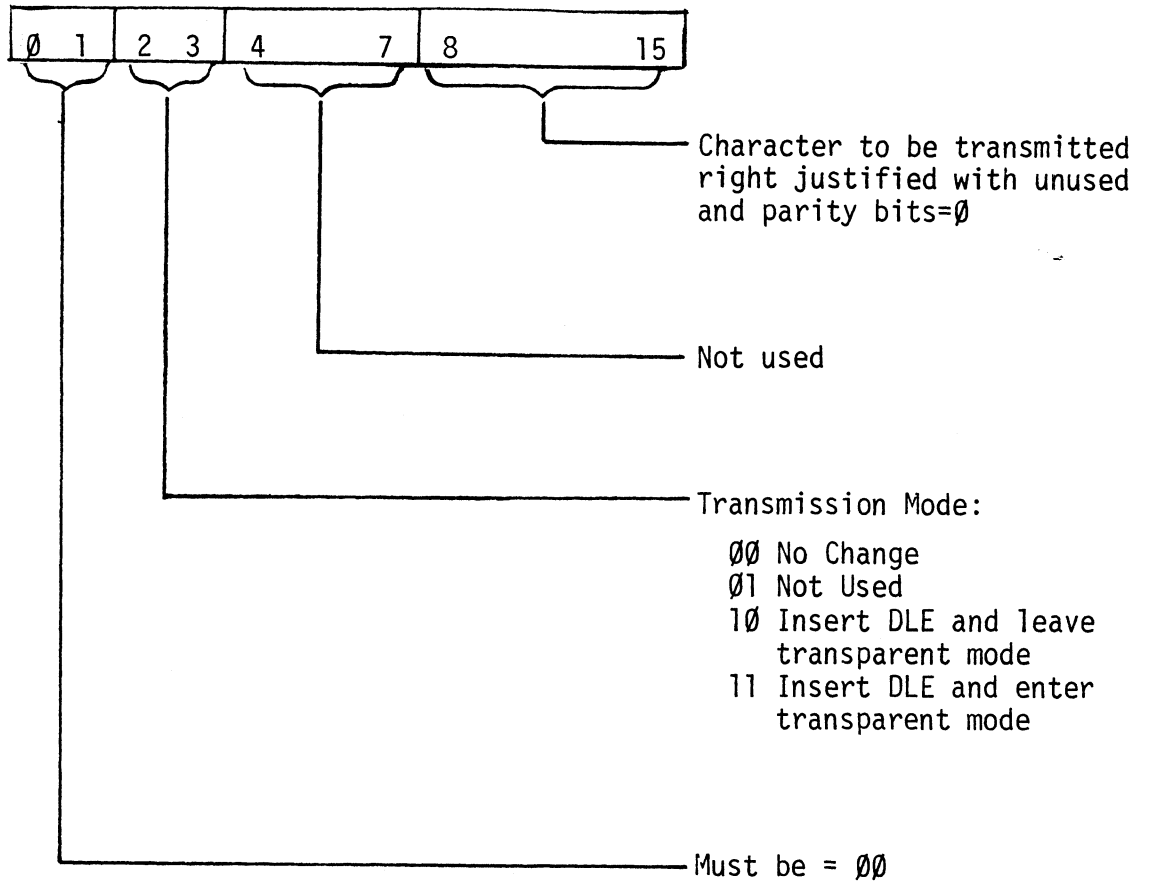
5.0 PROGRAMMING NOTES (cont.)

3) Transmit Underrun Sequence
    DOB (f) AC, MUX

```
┌───┬──────────────────────────┐
│Ø 1│2                       15│
└───┴──────────────────────────┘
```

Not Used

Must be = Ø1
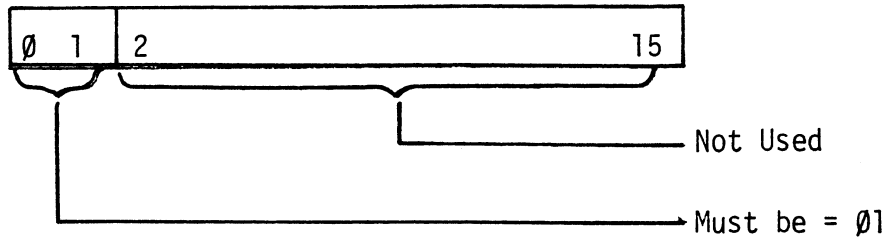
4) Set Modem Control Status
    DOB (f) AC, MUX

```
┌───┬─────────────┬──┬──┬──┬──┐
│Ø 1│2         11 │12│13│14│15│
└───┴─────────────┴──┴──┴──┴──┘
```

Modem Control Signals
(Ø=Off, 1=On)

Data Terminal Ready

Request to Send

Test 2

For test purposes;
May be user-defined

Test 1

Not Used

Must be = 1Ø
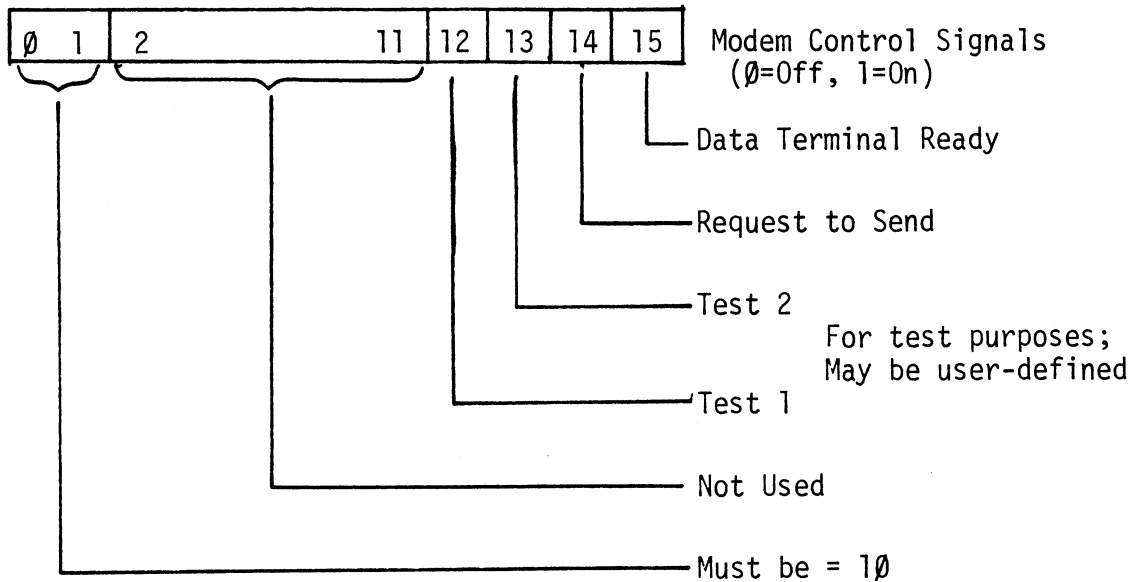
5.0   PROGRAMMING NOTES (cont.)

5) Control Line Section
    DOC (f) AC, MUX

| 0 1 | 2 ... 14 | 15 |

- Control Current Line/Section 0=Off, 1=On
- Not Used
- Must Be=00
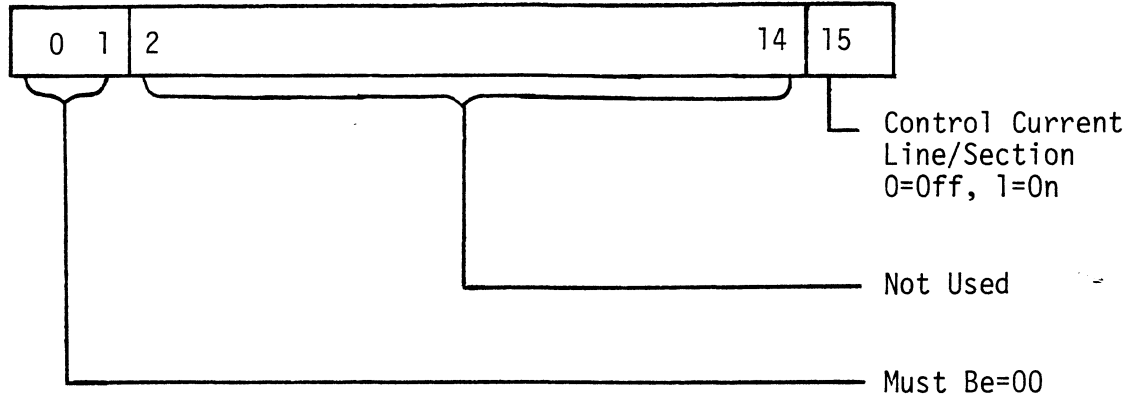
5.0 PROGRAMMING NOTES (cont.)

6) Set SYN Character
   DOC (f) AC, MUX

```
| 0    1 | 2        7 | 8          15 |
```

SYN Character for current
line/section, right-justified
with unused and parity bits
=0

Not Used

Must Be=01
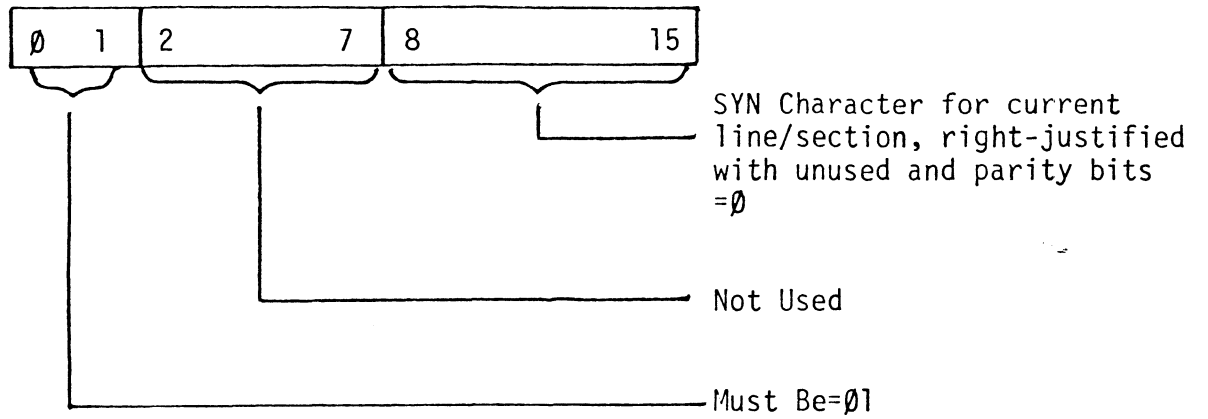
5.0 PROGRAMMING NOTES (cont.)

7) Specify Line Characteristics
   DOC (f) AC, MUX

Ø	1	2	5	6	7	10	11	12	13	14	15

Loopback: Ø=Off, 1=On

Parity: ØØ=No parity
        Ø1=Odd parity
        1Ø=Even parity
        11=Not Used

Word Length (Including parity)
        ØØ=Not Used
        Ø1=6 Bits
        1Ø=7 Bits
        11=8 Bits

Not Used

CRC Polynomial:
        Ø=CRC-16
          $(x^{16}+x^{15}+x^2+1)$
        1=CRC-CCITT
          $(x^{16}+x^{12}+x^5+1)$

Not Used

Must Be=1Ø
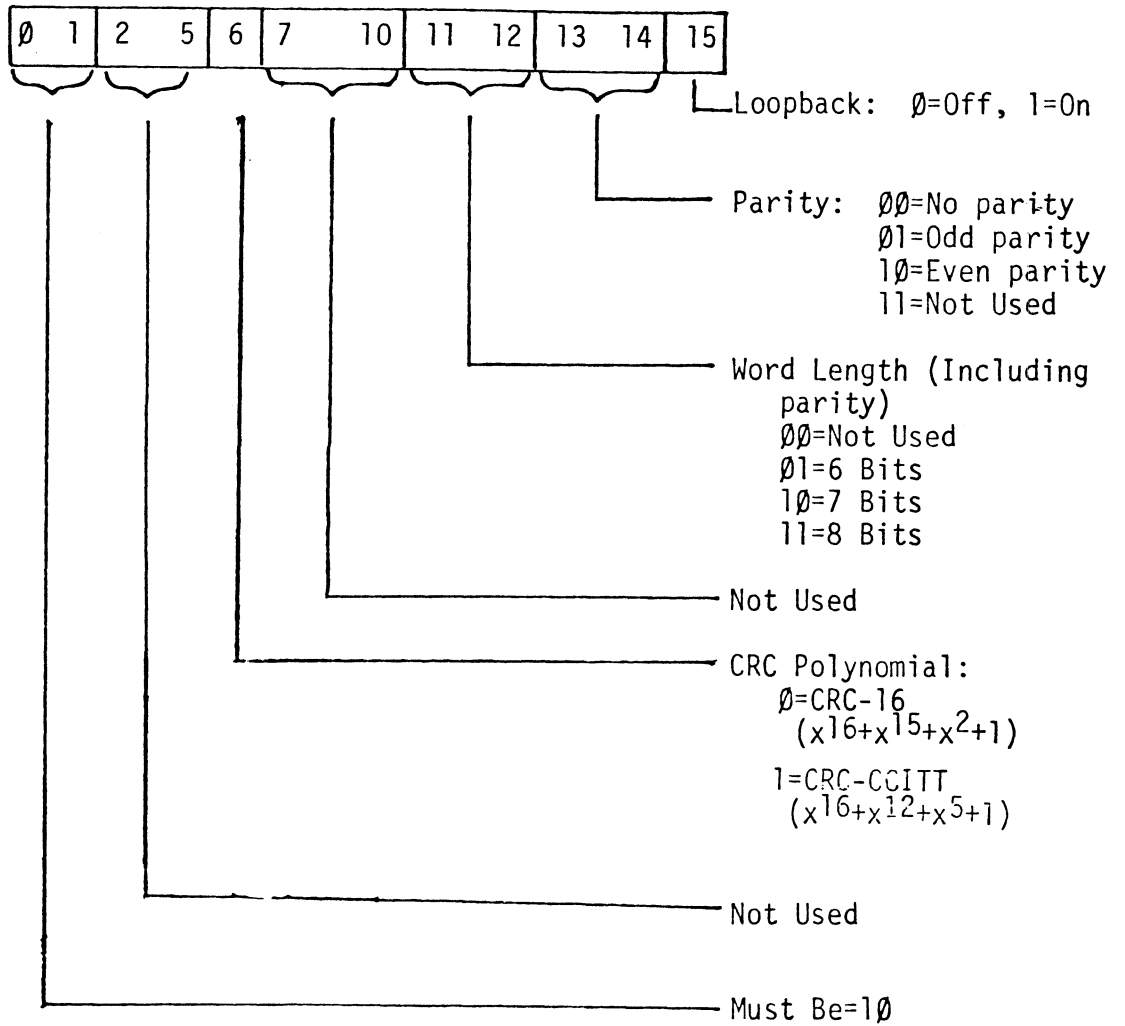
5.0 PROGRAMMING NOTES (cont.)

8) Set DLE Character (Transmitter only)
   DOC (f) AC, MUX

```
┌──┬──┬─────────┬───────────────┐
│Ø │ 1│2       7│8            15 │
└──┴──┴─────────┴───────────────┘
```

DLE character for current transmitter section, right-justified with unused and parity bits=Ø

Not Used

Must BE=11
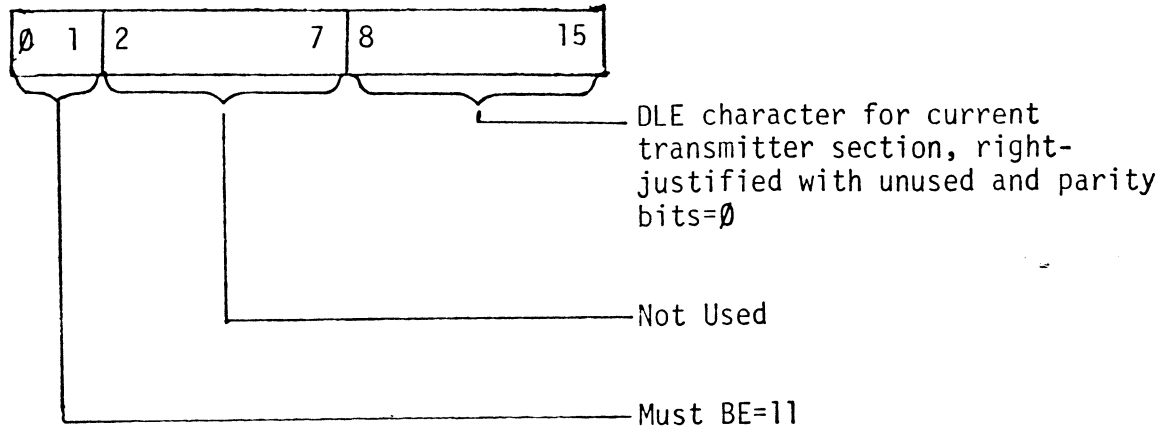
9) Read Line and Section Requesting Service
   DIA (f) AC, MUX

```
┌──────────┬──────────┬──┐
│Ø        6│7       14│15│
└──────────┴──────────┴──┘
```

Section: Ø=Receiver or Modem
1=Transmitter

Line Address: Ø-377$_8$

Not Used
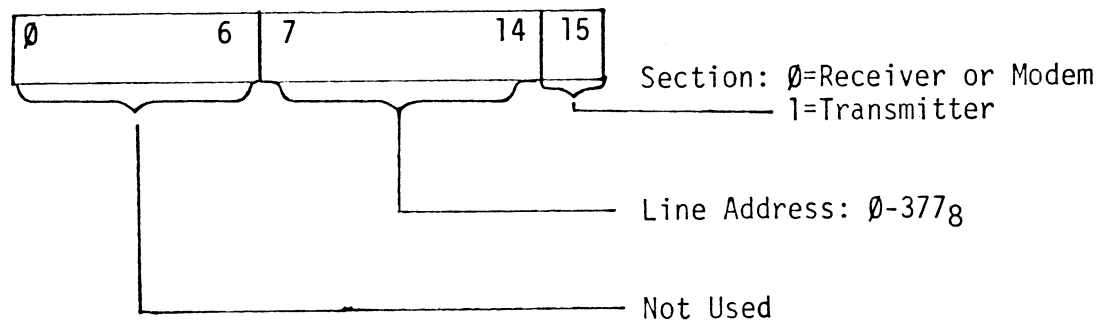
5.0 PROGRAMMING NOTES (cont.)

10) Read Received Data
     DIB (f) AC, MUX

0	7	8	15

Received character, right-justified with parity.

Not Used
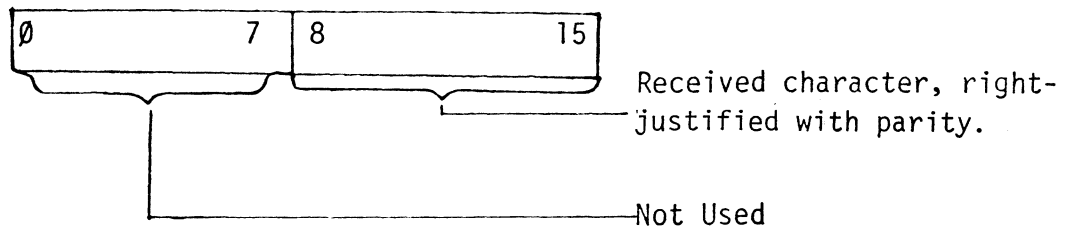
11) Read Receiver Status
     DIC (f) AC, MUX

0	10	11	12	13	14	15

Section: 0=Receiver

Overrun error=1

Parity error=1

Diagnostic data (offline only)
Bit 11=Transmit clock state
Bit 12=Transmit data state

Not Used
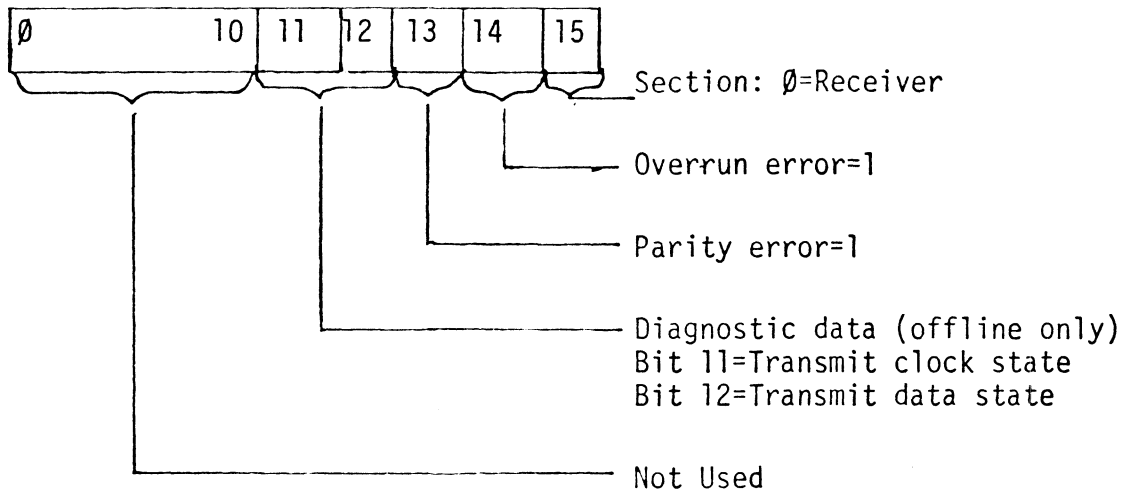
5.0 PROGRAMMING NOTES (cont.)

12) Read Modem Status
    DIC (f) AC, MUX
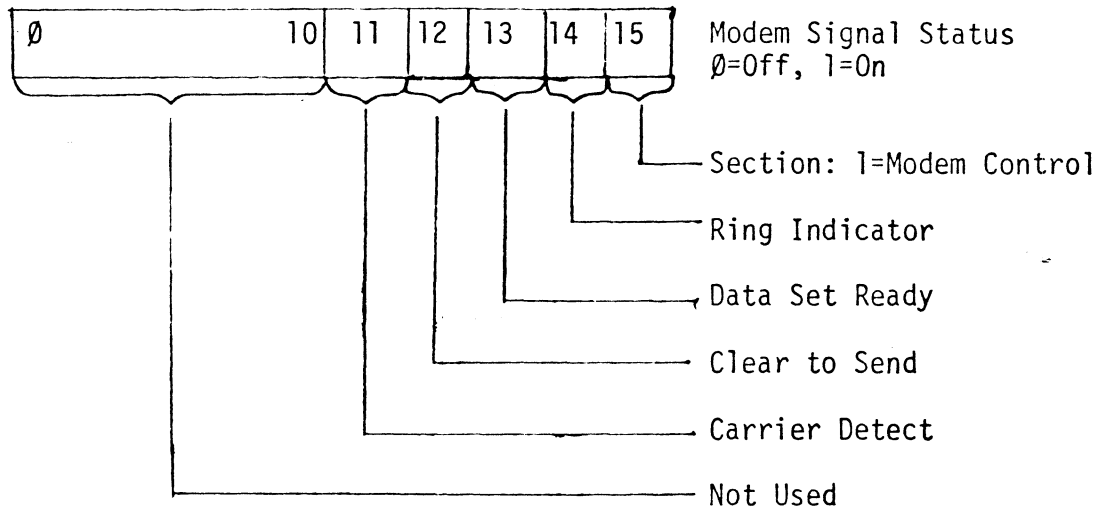
13) Load CRC Partial Result
    DOB (f) AC, CRC

14) Read CRC Partial Result
    DIB (f) AC, CRC
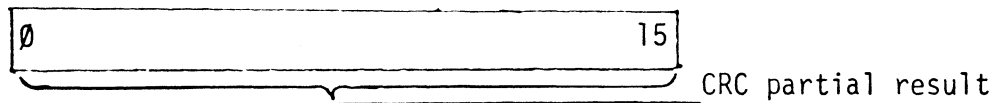
6.0 APPLICATION INFORMATION

6.1 SERIAL INTERFACE

The 25S connector on the internal cable provides serial interface for the PSI. The connector's pin assignments are standard EIA RS-232C and can be found in Section 7.3.
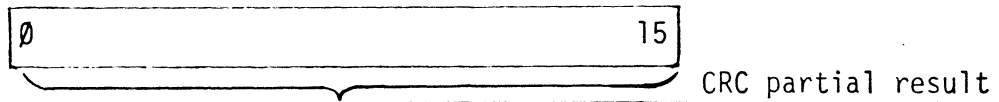
6.1.1   MODEM CONNECTION

Connection to synchronous modems using a 25S connector for digital inter-face is accomplished using a standard pin to pin cable with 25P connectors on each end (# 300-056-00, available as option). If the modem is externally clocked, be sure that the Local Clock on the PSI is set to provide the proper speed (Section 3.4).

6.1.2 DIRECT DATA LINK

Limited distance direct data links may be made between two synchronous line interfaces by using a modified cable. The signal connections for linking two PSI lines in full-duplex over a direct data link is shown in Figure 6.1 on the following page.

```
Transmitted Data 2 >─────────┼──────────►<3 Received Data
   Received Data 3 >◄─────────┼───────────<2 Transmitted Data
  Request to Send 4 >─────────┼──────────►<8 Carrier Detect
    Clear to Send 5 >◄────────┘          │
   Carrier Detect 8 >◄────────┼──┐        <4 Request To Send
                              │  └───────►<5 Clear To Send
Data Terminal Ready 20 >──────┼──────────►<6 Data Set Ready
   Ring Indicator 22 >◄───────┘          │
    Data Set Ready 6 >◄───────┼──┐        <20 Data Terminal Ready
                              │  └───────►<22 Ring Indicator
 Local Clock Out 24 >─────────┼──────────►<17 Receive Clock
 Transmit Clock 15 >◄─────────┘          │
   Receive Clock 17 >◄────────┼──┐        <24 Local Clock Out
                              │  └───────►<15 Transmit Clcok
  Signal Ground 7 >───────────┼──────────<7 Signal Ground

25 Pin
Connector Number ─┘
```
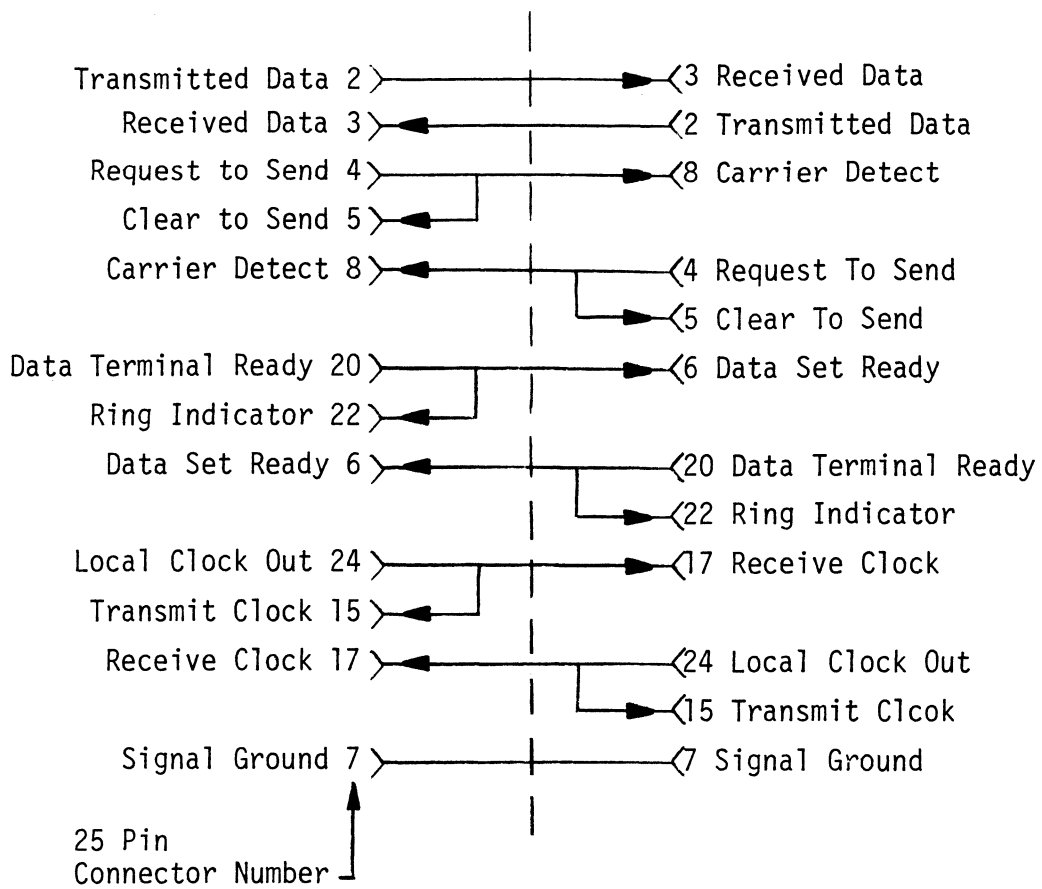
Figure 6.1

Signal Connections for directly connecting
two PSI lines

6.2   USING MULTIPLE PSI/PTI BOARDS

6.2.1 GENERAL

In systems which require more synchronous lines than are provided by
the controller, or in systems in which asynchronous in addition to sync
lines are needed, additional controller boards may be installed and use
the same device code. However, system limitations must be considered,
and inter-board priority must be established.

Although the total number of communication lines available per device
code is 256, due to system limitations the number of useable lines
may be less. Considerations must be taken as to the number of sync and
async lines the system allows, line address requirements, and maximum
allowable transfer rates before overruns occur.

Custom Systems offers a multi-line async controller that may be used
with the PSI/1-2. The Model 420 Programmable Terminal Interface (PTI)
provides async control of up to sixteen display terminals, serial
printers, or Bell 103 modems.

6.2.2 ADDRESSING

Because all lines use the same device code, each board must be set to
distinguish its lines from lines on other boards. Usually, the higher
the priority of a board, the lower its line address. Sync lines should
be given priority over async lines. For example, a system using one
PSI/2 and two PTI controllers may have the PSI/2 set for line addresses
0-1, one PTI set to 20_8 - 37_8, and the second PTI set to 40_8 - 57_8.

6.2.3 INTER-BOARD PRIORITY

The boards should be placed in the chassis with highest priority board
closest to the communication processor (either CPU or DCU), and the
second highest priority board in the next slot, etc. Also, a Data-In-A
priority scheme must be established between the board as follows:

- For systems using the CPU as communications processor, connect a jumper
  from backpanel Pin A83 (PRI-OUT) of the highest priority board (closest
  to the processor) to Pin A84 of the next lower priority board. Then
  connect Pin A83 of that board to Pin A84 of the next board. Repeat for
  all PSI and/or PTI boards in the chassis.

- For systems using a DCU as communications processor, jumpering is
  provided by the DCU backpanel jumper plugs. See Section 3.1 for
  installation and Section 12 for wiring specifications.

7.0   INTERFACING

7.1   INTERFACE SIGNALS (CPU)

SIGNAL NAME	ACTIVE LEVEL	PIN NUMBERS
Data 0	L	B62
Data 1	L	B65
Data 2	L	B82
Data 3	L	B73
Data 4	L	B61
Data 5	L	B57
Data 6	L	B95
Data 7	L	B55
Data 8	L	B60
Data 9	L	B63
Data 10	L	B75
Data 11	L	B58
Data 12	L	B59
Data 13	L	B64
Data 14	L	B56
Data 15	L	B66
DS0	L	A72
DS1	L	A68
DS2	L	A66
DS3	L	A46
DS4	L	A62
DS5	L	A64
DATIA	H	A44
DATIB	H	A42
DATIC	H	A54
DATOA	H	A58
DATOB	H	A56
DATOC	H	A48
START	H	A52
CLEAR	H	A50

7.1 INTERFACE SIGNALS (CPU) (cont.)

SIGNAL NAME	ACTIVE LEVEL	PIN NUMBERS
INTA	H	A40
IOPLS	H	A74
IORST	H	A70
MASKO	L	A38
RQENB	L	B41
INTR	L	B29
SELB	L	A82
SELD	L	A80
INTP-IN	L	A96
INTP-OUT	L	A95
DCHP-IN	L	A94
DCHP-OUT	L	A93

7.2 INTERFACE SIGNALS (DCU)

DDATA 0	L	A69
DDATA 1	L	A75
DDATA 2	L	A91
DDATA 3	L	A77
DDATA 4	L	A67
DDATA 5	L	A59
DDATA 6	L	A92
DDATA 7	L	A47
DDATA 8	L	A65
DDATA 9	L	A71
DDATA 10	L	A78
DDATA 11	L	A61
DDATA 12	L	A63
DDATA 13	L	A73
DDATA 14	L	A57
DDATA 15	L	A76

7.2 INTERFACE SIGNALS (DCU) (cont.)

SIGNAL NAME	ACTIVE LEVEL	PIN NUMBER
DDS0	L	B13
DDS1	L	B19
DDS2	L	B23
DDS3	L	B51
DDS4	L	B27
DDS5	L	B25
DDATIA	H	B52
DDATIB	H	B53
DDATIC	H	B38
DDATOA	H	B34
DDATOB	H	B36
DDATOC	H	B49
DSTART	H	B40
DCLEAR	H	B48
DINTA	H	B54
DIOPLS	H	B11
DIORST	H	B15
DMASKO	L	B67
DRQENB	L	A49
DINTR	L	A86
DSELB	L	A90
DSELD	L	B6
DINTP-IN	L	A87
DINTP -OUT	L	A89

COMMON SIGNALS:

PRI-IN	H	A84
PRI-OUT	H	A83

7.3 SERIAL INTERFACE SIGNALS

(Pin numbers and names are the same for both lines)

SIGNAL NAME	25S CONN. PIN #	HEADER CONN. PIN #
*Protective Ground	1	1
Transmitted Data	2	3
Received Data	3	5
Request to Send	4	7
Clear to Send	5	9
Data Set Ready	6	11
Signal Ground	7	13
Carrier Detect	8	15
Test 1	11	21
Transmit Clock	15	4
Receive Clock	17	8
Test 2	18	10
Data Terminal Ready	20	14
Ring Indicator	22	18
Local Clock Out	24	22

*Boards initially have no connection to Protective Ground. To connect
Protective Grand to Signal Ground, insert a jumper into J17-1, located
near chip loc. A1Ø.

8.0 SPECIFICATIONS

POWER REQUIREMENTS

Power is supplied by the chassis +5 Volt and either the +15 Volt or +12 Volt power supplies.

+5 Volt current	= 2.5A Max
+12 or +15 Volt current	= 50MA Max

SERIAL INTERFACE

Communication with the modem is in accordance with EIA Standard RS-232C signal levels.

Transmit
Mark	-12 Volts Nominal
Space	+12 Volts Nominal

Receive
Mark	- 3 to -25 Volts
Space	+ 3 to +25 Volts

ENVIRONMENTAL

Operating Temperature	10^oC to 40^oC
Operating Humidity	10% to 90% NC
Non-operating Temperature	-40^oC to 55^oC
Non-operating Humidity	10% to 90%

9.0   DIAGNOSTIC TESTING

A diagnostic tape (400-247-00) is provided with the PSI which contains
diagnostic and reliability tests for testing the controller board.
If a problem is suspected, the reliability test should be run to
determine if a problem exists in the controller circuitry.

The tape is 9 track, 800 bpi (bits per inch) with a "T-BOOT" loader.

9.1   LOADING AND RUNNING TESTS

With the tape loaded on the drive and ready (at load point) initiate
a program-load from the tape drive unit. A menu of the contents of the
tape should be displayed. Enter the file number of the test to be
run followed by a carriage-return. A description of the tests on files
may be found at the end of this Section.

The tests begin by asking the operator questions pertaining to hardware
configuration such as controller model, device code, line address,
processor type, etc. These parameters should be verified before testing.

For PSI/1-2 boards the reliability test PMUX RELI is used. This test
requires no hardware modification or test plug, however, a test plug must
be used if modem control is to be tested. Test plug information is found
in the listing Section which follows. Once the test is running, status
is periodically displayed which shows the number of successful passes of
individual tests, and the total number of errors. If an error occurs
a brief description of the error is displayed. If excessive errors occur,
re-check hardware configuration. If errors still exist, the diagnostic
test may be run to help isolate the specific problem.

NOTE: Maximum operating speed of the reliability test may vary depending
on the speed of the processor used. If excessive overruns occur, reduce
the local clock speed to 4800 baud or less.

9.1   LOADING AND RUNNING TEST (cont.)

The diagnostic test PSI DIAG may be run to help isolate a problem. A
test plug is required which terminates the ribbon cable when running
the diagnostic test. Test plug information is found in the following
Section. For dual line boards (PSI/2), the test plug is jumper connecting
Line 0 to Line 1. If no errors occur, "PASS..." will be displayed. If
an error occurs, the program count of the error will be displayed and the
test will loop on the error. A description of the error may be found
by locating the program count in the listing Section which follows.

MAG TAPE 400-247-00

File 0 - T-BOOT loader program
File 1 - Directory - list of files on tape
File 2 - PSI DIAG - diagnostic program for testing the PSI. ②
File 3 - PMUX RELI - reliability test for PSI/1 or PSI/2 type
           boards. ①
File 4 - UMUX RELI - reliability test for PSI/U type boards.①
File 5 - The previous save files in dump format for storage on-disk.

NOTE 1: If for any reason the reliability tests cannot be loaded and
         run, Data General's 4200 RELI and 4243R tests may be run as
         alternatives for PMUX RELI and UMUX RELI, respectively.

NOTE 2: To run the PSI DIAG test, a test plug must be used to terminate
         the 25S connector of the ribbon cable. See the listing header
         in the next section for plug specifications.

ZETA ⟟⟐

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Problems will be promptly addressed and action taken as
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DOCUMENT NUMBER_____REVISION_____
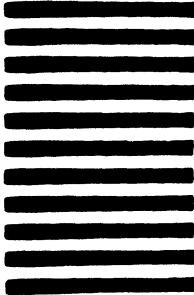

ERRORS IN MANUAL:

SUGGESTIONS FOR IMPROVING EITHER THE MANUAL OR THE PRODUCT:

BUSINESS REPLY MAIL
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ZETA⊂O

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