LOTUS 700

DISC CONTROLLER
USER MANUAL

POINT 4
DATA CORPORATION

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2569 McCabe Way / Irvine, California 92714

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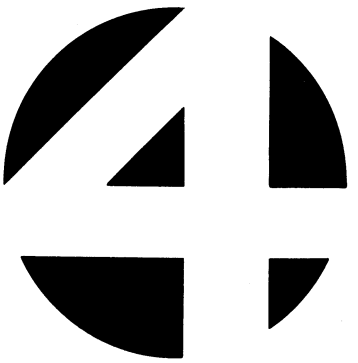

NOTICE

Every attempt has been made to make this reference manual complete, accurate and up-to-date. However, all information herein is subject to change due to updates. All inquiries concerning this manual should be directed to POINT 4 Data Corporation.

POINT 4 Data Corporation
2569 McCabe Way
Irvine, CA 92714
(714) 863-1111

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Changes, additions, and deletions to information in this manual are indicated by vertical bars in the margins or by a dot near the page number if the entire page is affected. A vertical bar by the page number indicates pagination rather than content has changed.

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PREFACE

This manual is for use by the system installation technician and the system programmer involved in the installation and software integration of the LOTUS 700 Disc Controller into a minicomputer system.

It includes features, hardware characteristics, installation procedures, configuration PROM coding, I/O instruction programming, and disc controller commands. Disc controller register functions, accumulator bit usage, disc controller commands, and controller and drive status bits are given in tabular form for ease of reference.

The appendices include a summary of accumulator formats and configuration chart examples.

Related manuals include:

Title	Document Number
POINT 4 User Reference Manual	HM-080-0003
LOTUS 700 Disc Controller Utilities and Diagnostics Manual	HM-121-0016

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Section 1
INTRODUCTION

1.1 GENERAL DESCRIPTION

POINT 4 Data Corporation's LOTUS 700 Disc Controller offers economical, high-performance moving-head disc storage interface for the POINT 4 Computer and NOVA*-type minicomputer systems. The single-board design uses low-power Shottky and MSI logic, providing the highest level of performance and reliability. The controller occupies one slot in the processor chassis and all connections to the drives are made directly from the disc controller board.

The LOTUS 700 Disc Controller interfaces up to four storage module-type drives, at transfer rates up to 1.2 megabytes per second. Drives supported include: the CDC 9448, 9730, and 9760 series; Ampex; Century Data; Okidata; Kennedy and Fujitsu. The four possible drives interfaced may be a mixture of any of the drives supported. Automatic program load is always from the lowest-numbered, ready drive unit.

Data to or from computer memory is transferred in two-byte words using the Direct Memory Access (DMA) Data Channel of the computer. The 9.67 MHz drive data transfer rate translates into 1.209 megabytes per second or 1.65 microseconds per DMA cycle at the computer. The computer must be able to support this DMA transfer rate. An 18-word FIFO buffer is used to prevent Data Late conditions.

The LOTUS 700 Controller is software-compatible with the IRIS (Interactive Real-time Information System) Operating System used on the POINT 4 and many NOVA-type computers. Four data-out instructions supply the controller with information required to perform any operation. Sixteen operations (including read/write/verify, seek and disc formatting) may be specified using controller commands. Seven data-in instructions obtain status information from the controller. Disk utility and diagnostic programs are provided.

Figure 1-1 is a photograph of the LOTUS 700 Disc Controller.

*NOVA is a trademark of Data General Corporation

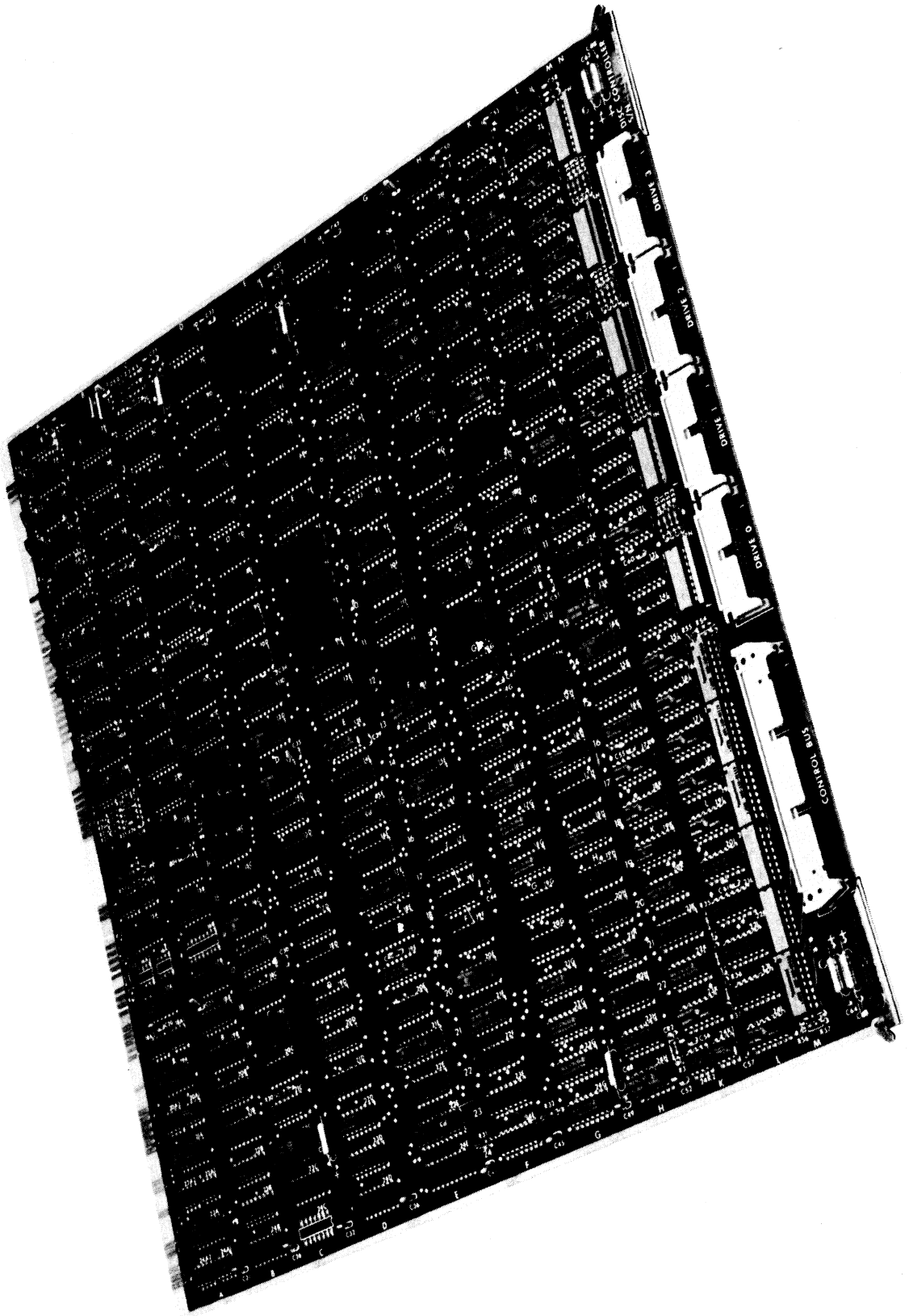

Figure 1-1. LOTUS 700 Disc Controller Board

1.1.1 Features

Many features make the LOTUS 700 Disc Controller a valuable addition to a POINT 4 Computer system. Compatibility, reliability, flexibility and advanced design are apparent in the following features:

- POINT 4 Computer I/O bus-compatible
- IRIS Operating System-compatible
- Interfaces up to four storage module-type drives in any combination
- Data transfer rate of 1.209 megabytes per second
- Whole track transfer in a single operation
- Format routine included in controller logic
- Overlapped seek
- 32-bit ECC error detection and provision for software correction
- Bad and alternate sectoring flags
- Supports dual port drives interfacing to two computers
- Built-in reliability and maintenance features
- Disc utility and diagnostic programs

1.1.2 Disc Controller Operation

The computer uses I/O instructions to transfer information between the processor's general purpose 16-bit accumulators and registers in the LOTUS 700 Disc Controller. Information transferred may be commands, computer memory addresses, disc addresses, controller or drive status, or ECCR codes. From this information the controller initiates seeks, reads and writes to and from the drive.

Addressing capacity per drive is 1024 tracks, 32 surfaces, and 32 sectors. Each sector contains 512 bytes of data. Up to 32 consecutive sectors may be transferred per operation with the cylinder boundary being crossed if necessary.

Hardware alternate sectoring and automatic retry are switch-selectable. Bad sector and alternate sector flags are provided to point out sectors known to be faulty. These flags are set during disc formatting. If the alternate sector flag is set, the alternate sector address is specified in the sector header. Alternate sectoring is done automatically requiring no program intervention.

Overlapped seek allows simultaneous seek and data transfers on multi-drive systems. Once a seek command has been issued to the drive, the LOTUS 700 Controller is ready to accept another command from the CPU. When the data transfer command is completed, a program interrupt request is issued to alert the CPU of the completed transfer.

Additional features include a 32-bit ECC error detection code for read or write operations. Error correction is programmable. In addition, system flexibility is increased by use of a programmable device code.

1.2 INPUT/OUTPUT INTERFACE

The LOTUS 700 Controller is designed to operate on POINT 4 and NOVA-type computers which are compatible with the specifications listed under Computer Interface. Disc drives controlled by the LOTUS 700 Controller operate under the specifications listed under Disc Drive Interface.

COMPUTER INTERFACE	
I/O Bus	POINT 4 and NOVA-type Computer I/O bus-compatible
Backplane wiring	None required
I/O bus loading	Single 7400-type input load; Single 75453-type output driver
Device Code	Programmable
Priority mask bit	7; 8 is optional
DMA transfer rate	1.209 Megabytes/sec (1.65 microsecond/DMA cycle)**
DISC DRIVE INTERFACE	
Type of interface	Storage module drive-compatible
Drives per controller	4 maximum
Drive type and size	Any mixture
Number of surfaces per drive	32 maximum*
Number of tracks per surface	1024 maximum*
Number of sectors per track	32 maximum*
Data transfer rate	9.67 MHz maximum**
Access time	1/2 revolution average, 1 revolution maximum*
Sector size: Header	6 bytes + 2 bytes of CRC
Data	512 bytes + 4 bytes of ECC
Number of consecutive sectors transferable in one operation	32 maximum
Bad sector flag	1st bit of header
Alternate sector flag	2nd bit of header
Alternate sector location	Any; specified in header
Program load	From lowest numbered ready drive
FIFO buffer size	18 words
Overlap seek execution	Yes
Alternate sectoring	Yes
ECC error detection	Yes
ECC error correction	Provision for software correction

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* Function of Disc Drive
**From SMD Specification

1.3 SPECIFICATIONS

POINT 4 Data Corporation's LOTUS 700 Disc Controller package includes: the 700 Controller board, the cable set to the first drive, a disc utility program for formatting and surface analysis, and a diagnostic program. Physical, electrical and environmental specifications for the controller follow:

PHYSICAL	
700 Dimensions	Single board, 15"x15"
Cabling to drives	A Cable: 30-pair control bus; daisy-chained; terminated at last drive B Cables: 26-wire flat cable; radial; one per drive
Cable Connector	Located at front of controller board
POWER REQUIREMENTS (maximum)	
Current	+5 ±5%, 3.8A maximum -5 ±5%, 0.8A maximum
Power	23W
OPERATING ENVIRONMENT	
Operating Temperature	0-55C
Relative Humidity	0-90% noncondensing

Section 2
HARDWARE INTERFACE

2.1 INTRODUCTION

This section covers those hardware characteristics for which an understanding is essential to the user for installation and programming of the LOTUS 700 Controller. Covered in this section are:

- Controller architecture
- Controller registers used in I/O programming
- Installation and cabling
- Input/Output cable signal charts
- Hardware-selectable options
- Disc I/O system configuration

2.2 LOTUS 700 CONTROLLER ARCHITECTURE

The LOTUS 700 Controller serves as an interface between the processor and up to four disc drives. Figure 2-1 is a block diagram of the 700 Controller logic.

Interface to the processor is via the processor I/O DMA bus. Information passed between the processor and the controller includes:

- Data
- DMA transfer control signals
- Status information
- I/O instructions
- Device select signals

Internal processing which must take place within the controller includes:

- Command decoding
- Memory addressing
- Data buffering
- ECC code generation
- Head and sector PROM decoding
- Cylinder/alternate cylinder addressing
- Controller and drive status
- Controller storage registers
- Word and sector counting
- Header, data and sector comparison
- Sync detection
- Seek status detectors

Interface to the disc drives is via the Drive Cables (B) and the Control Bus Cables (A). Drivers and receivers control transfer of signals from each drive cable and the Control Bus to internal controller logic.

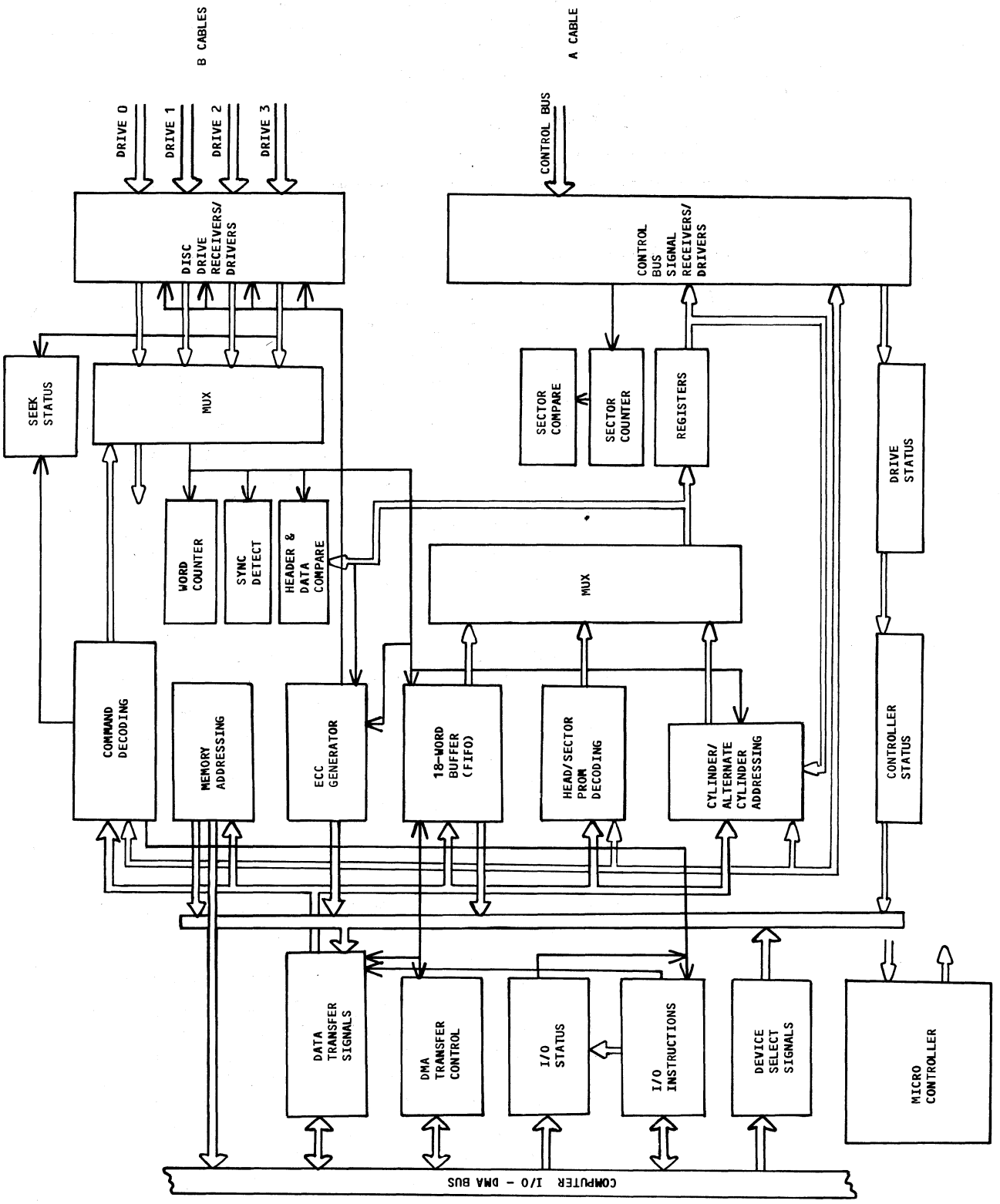


Figure 2-1. LOTUS 700 Disc Controller Block Diagram

2.2.1 Controller Registers

The LOTUS 700 Controller has a series of registers which are used for storage of information pertinent to the data transfer operation. This information includes addresses, status, commands, and the error correction code remainder. These registers perform important functions during the transfer of information in and out of the processor via I/O instructions. The registers and their functions are listed below.

Register	No. of Bits	Function
COMMAND	4	Holds the disc controller command, specified in bits 5-8 of the specified processor accumulator. The command is transferred to the controller by the DOA (Specify Drive and Command) instruction. There are 16 commands which control disk drive operation, ranging from 0000 to 1111 in bit arrangement. See Section 3.2.1 for specific descriptions of controller commands.
DRIVE ADDRESS	2	Holds the disc drive address, specified in bits 9 and 10 of the specified processor accumulator. The drive address is transferred to the controller by the DOA (Specify Drive and Command) instruction. The drive address is a two-bit programmable number. Only four drives may be connected to one LOTUS 700 Disc Controller.
MEMORY ADDRESS	16	Holds the processor memory address to which or from which the data transfer will take place. The 16-bit address is transferred to the controller's Address Register from the specified processor accumulator by the DOB (Specify Memory Address) instructions. The DIA instruction in Alternate Mode 1 reads the memory address from the Memory Address Register into the specified processor accumulator.

Register	No. of Bits	Function
CYLINDER ADDRESS	10	Holds the disc sector address of the sector involved in the data transfer operation. This address is transferred into the controller's Cylinder Address Register from bits 6-15 of the specified processor accumulator by the DOC (Specify Cylinder) instruction when a seek command has been specified by the previous instruction.
VOLUME	1	Holds the volume select bit which defines the non-removable surface(s) in CMD drives. This bit is transferred into the controller's Volume Register from bit 11 of the specified processor accumulator by the DOA (Specify Command and Drive) instruction, if the drive addressed is a CMD drive.
SURFACE ADDRESS	5	Holds the surface address of the sector involved in the data transfer. This address is transferred into the controller's Surface Address Register from bits 1-5 of the specified processor accumulator by the DOC instruction when the previous DOA instruction specified other than a seek command. This address is read from the Surface Address register into bits 1-5 of the specified processor accumulator by the DIC instruction.

Register	No. of Bits	Function
SECTOR ADDRESS	5	Holds the sector address of the sector involved in the data transfer. The sector address is transferred into the controller's Sector Address Register from bits 5-10 of the specified processor accumulator by the DOC instruction if the previous DOA instruction specified other than a seek command. This address is read from the Surface Address Register into bits 5-10 of the specified processor accumulator by the DIC instruction.
SECTOR COUNT	5	Holds the two's complement of the number of sectors to be transferred. The sector count is transferred into the controller's Sector Count Register from bits 11-15 of the specified processor accumulator by the DOC instruction if the previous DOA instruction specified other than a seek command. The sector count is read from the Sector Count Register into bits 11-15 of the specified processor accumulator by the DIC instruction.
ECCR	32	Holds the 32-bit error correction code remainder (ECCR) which is used to detect and correct certain data errors. The high-order 16 bits of the controller's ECCR Register are read into the specified processor accumulator by a DIA instruction in Alternate Mode 2. The low-order 16 bits of the controller's ECCR Register are loaded into the specified processor accumulator by a DIB instruction in Alternate Mode 2.

Register	No. of Bits	Function
CONTROLLER STATUS	15	Holds the controller's status flags. There are 15 flags which, when set to one (1), identify error conditions related to data transfer operations. See Subsection 3.2.5.1 for descriptions of error conditions. The controller status information is read from the Controller Status Register into the specified processor accumulator by the DIA (Read Controller Status) instruction.
DRIVE STATUS	10	Holds the drive status information of the selected disc drive. There are four status flags and six error condition flags which are set to one (1) to report on drive status. See Subsections 3.2.7 and 3.2.7.1 for descriptions of status and error conditions. The drive status information is read from the controller's Drive Status Register to the specified processor accumulator by the DIB (Read Drive Status) instruction.
EXTENDED MEMORY ADDRESS (optional)	4	Holds the optional extended memory address used when memory mapping is required to access all of system memory. The DOB (Specify Memory Address) instruction causes the transfer of 4 bits of XMA information from the controller's Auxiliary Register into the Extended Memory Address Register. The DIB instruction in Alternate Mode 1 reads the XMA information from the controller's Extended Memory Address Register into bits 12-15 of the specified processor accumulator.

Register	No. of Bits	Function
AUXILIARY	4	The controller's Auxiliary Register is used for temporary storage of the XMA information transferred to the controller from bits 12-15 of the specified AC by the DOA (Specify Command and Drive) instruction until the memory address for the operation specified in the DOA instruction is transferred into the Memory Address Register. When the memory address is transferred to the controller by a DOB instruction the 4 XMA bits are transferred from the Auxiliary Register to the Extended Memory Address Register.

2.3 CONTROLLER INSTALLATION

The LOTUS 700 Controller is a single-board design occupying only one slot in the processor chassis. The disc controller normally occupies the slot nearest the CPU board in the processor chassis.

The controller board should be added to the chassis with caution, making sure the card edge connector slides smoothly into the backplane sockets. No backplane wiring is required.

Cabling between the controller board and the disc drives consists of a control bus daisy-chained between drives and a separate drive cable to each drive. Cable descriptions are as follows:

Cable	Function	Description
A	Control Bus	30-pair (60-pin) control bus, daisy-chained between drives, terminated at the last drive
B	Drive Cables	26-wire flat cable, radial one per drive

Connections to the controller are made at the front of the controller board.

One end of the Control Bus Cable mounts at the 60-pin connector on the front of the LOTUS 700 Controller board. The other end mounts to the control bus input connector on the first disc drive. If there is more than one drive on the system, control bus cables must be connected between the output connector on each drive and the input connector on the next drive. The output connector on the last drive must be fitted with a bus terminator.

Drive cables are connected on the LOTUS 700 board to the 26-pin connector adjacent to the Control Bus connector and the Drive 3 Cable at the 26-pin connector furthest from the Control Bus connector. The opposite end of the drive cables connect to the 26-pin drive connectors on each respective drive.

NOTE

A ground strap must be strung between the drives at the ground connector and attached to the computer chassis.

Figure 2-2 is an illustration of controller-to-drive cabling.

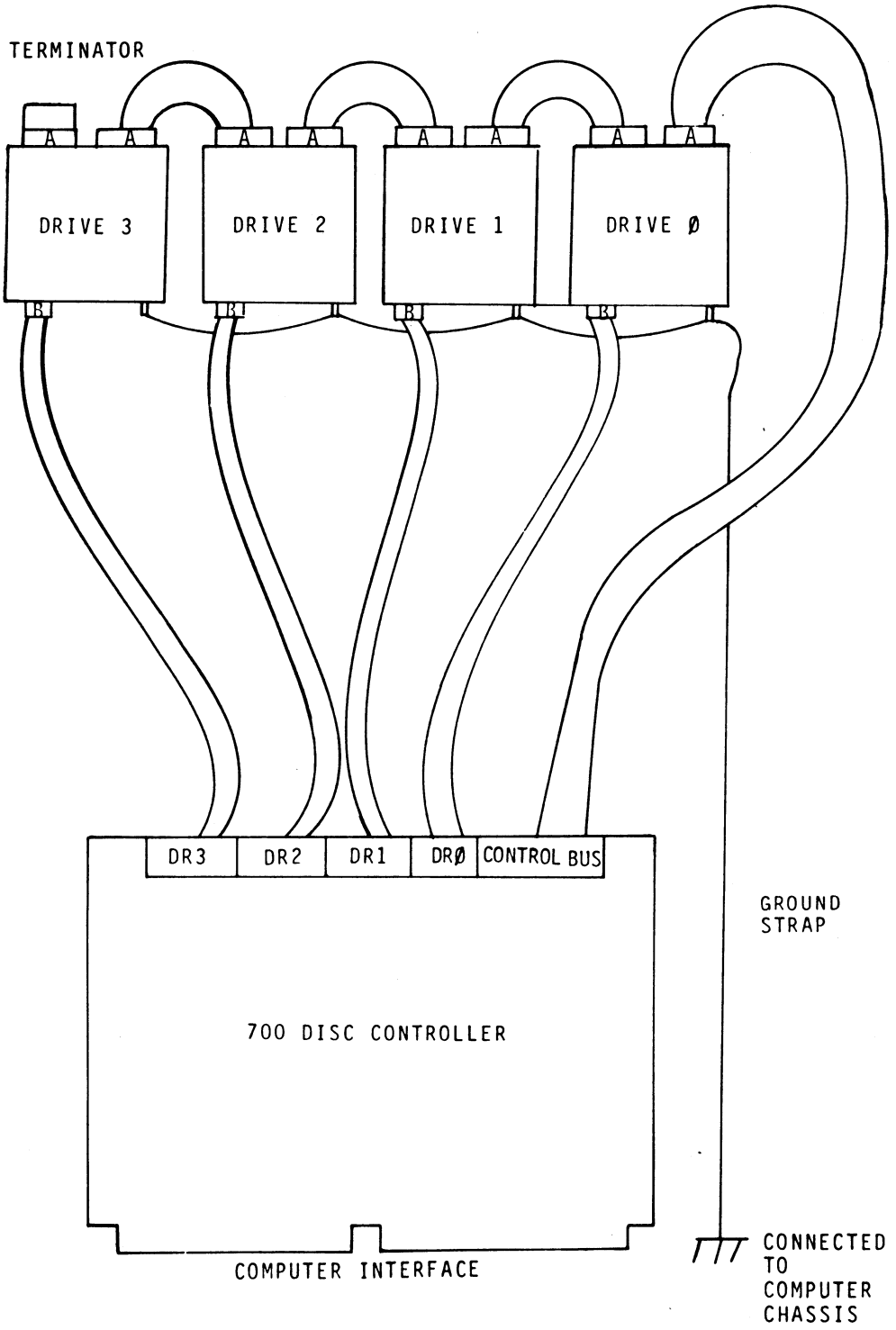


Figure 2-2. Controller-to-Drive Cabling

2.3.1 Cable Interface Signals

Successful system operation requires both that cabling is properly installed and that cable signals are properly configured. Tables 2-1 and 2-2 list signal configuration of the cables provided with the LOTUS 700 Controller. Check documentation provided with disc drives to be connected to the controller for verification that drive I/O interface signals correspond to control bus and drive cable connector signals.

Connector signal configurations are provided on the following tables:

Table 2-1. Control Bus Signals, A Cable

Table 2-2. Drive Cable Signals, B Cable

TABLE 2-1. CONTROL BUS SIGNALS
A CABLE

Controller/Drive 60-Pin Flat Cable Pin #	Signal Name	Optional 75-Pin Trailing Cable (available on some drives) Pin #
1 31	- + Tag 1	46 49
2 32	- + Tag 2	48 51
3 33	- + Tag 3	52 55
4 34	- + Bit 0	23 26
5 35	- + Bit 1	24 27
6 36	- + Bit 2	28 31
7 37	- + Bit 3	29 32
8 38	- + Bit 4	30 33
9 39	- + Bit 5	34 37
10 40	- + Bit 6	35 38
11 41	- + Bit 7	36 39
12 42	- + Bit 8	40 43
13 43	- + Bit 9	41 44
14 44	- + Open Cable Detect	16 20

Controller/Drive 60-Pin Flat Cable Pin #	Signal Name	Optional 75-Pin Trailing Cable (available on some drives) Pin #
15 45	- + Fault	11 14
16 46	- + Seek Error	75 78
17 47	- + On Cylinder	15 18
18 48	- + Index	10 13
19 49	- + Unit Ready	17 21
20 50	- + (Address Mark Found)	42 45
21 51	- + Unit Reserved (Busy)	47 50
22 52	- + Unit Select Tag	22 25
23 53	- + Unit Select 2^0	1 4
24 54	- + Unit Select 2^1	2 5
25 55	- + (Sector)	74 77
26 56	- + Unit Select 2^2	3 7
27 57	- + Unit Select 2^3	8 12
28 58	- + Write Protected	53 56
29 59	- PICK - HOLD	73 76
30 60	- + Spare	54 57

TABLE 2-2. DRIVE CABLE SIGNALS
B CABLE

Controller/Drive 26-Pin Flat Cable Pin #	Signal Name	Optional 32-pin Trailing Cable Pin #
1	GND	K
14 2	+ − Servo Clock	N M
15	GND	T
3 16	− + Read Data	U V
4	GND	Y
17 5	+ − Read Clock	X W
18	GND	E
6 19	− + Write Clock	H J
7	GND	D
20 8	+ − Write Data	B A
21	GND	C
9 22	+ − Unit Selected	BB DD
10 23	− + Seek End	AA CC
11	GND	LL
24 12	+ − (Index Mark)	HH EE
25	GND	NN
13 26	− + (Sector Mark)	FF JJ

2.4 HARDWARE-SELECTABLE OPTIONS

Three options are selectable via etch cuts/jumpering on the LOTUS 700 Controller board. These options are:

- Automatic Retry
- Mask Bit
- Device Address

Selection of these options is explained in the following subsections.

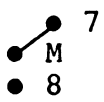
2.4.1 Automatic Retry Option

Automatic Retry after an unsuccessful seek operation is enabled by an etch located on the LOTUS 700 Controller board at coordinate C/9. It is identified by "RETRY" on the PC board. The two feed-through-holes to the right of RETRY are connected by an etch. This etch enables the Automatic Retry option. The option appears as follows on the PC board:

To disable this option, cut the etch.

2.4.2 Mask Bit Option

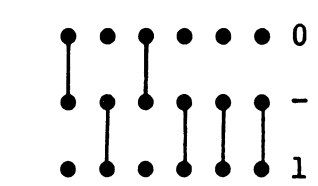
The LOTUS 700 Controller offers the option of using either bit 7 or bit 8 as the mask bit. Bit 7 is standard and bit 8 is optional. The mask bit option is located between column C and B and between rows 13 and 14. It is identified by an "M" on the PC board. The feed-through-hole directly to the left of the "M" enables the mask bit. It is etched to the feed-through-hole by the "7" as the mask bit. The option appears as follows on the PC board:



To select bit 8 as the mask bit, cut the etch between "7" and "M" and make a connection between "M" and "8".

2.4.3 Device Address Option

The device address for the 700 Controller is established by a 6-bit etch located at coordinate C/1 on the PC board. The existing etch on the delivered PC board is set to device code 27 (octal). The existing etch appears as follows:



To change the controller device address cut the existing etches and jumper the center feed-through-holes to 0 (zero) or 1 (one) as required for the new octal address.

2.5 DISC I/O SYSTEM CONFIGURATION

The LOTUS 700 Controller features flexibility in system configuration by allowing any mixture of compatible drives to be attached to a controller. This flexibility is made possible through the use of two configuration PROMs which must be programmed with control information for the attached drives.

The Head (Surface) PROM (22C on the 700 board) and the Sector PROM (19C on the 700 board) provide information within the controller about the type and size of the attached drives. These PROMs flag illegal surface and/or illegal sector numbers supplied by the CPU for data transfer operations. They also provide information on sector and/or surface overflow in multisector transfers.

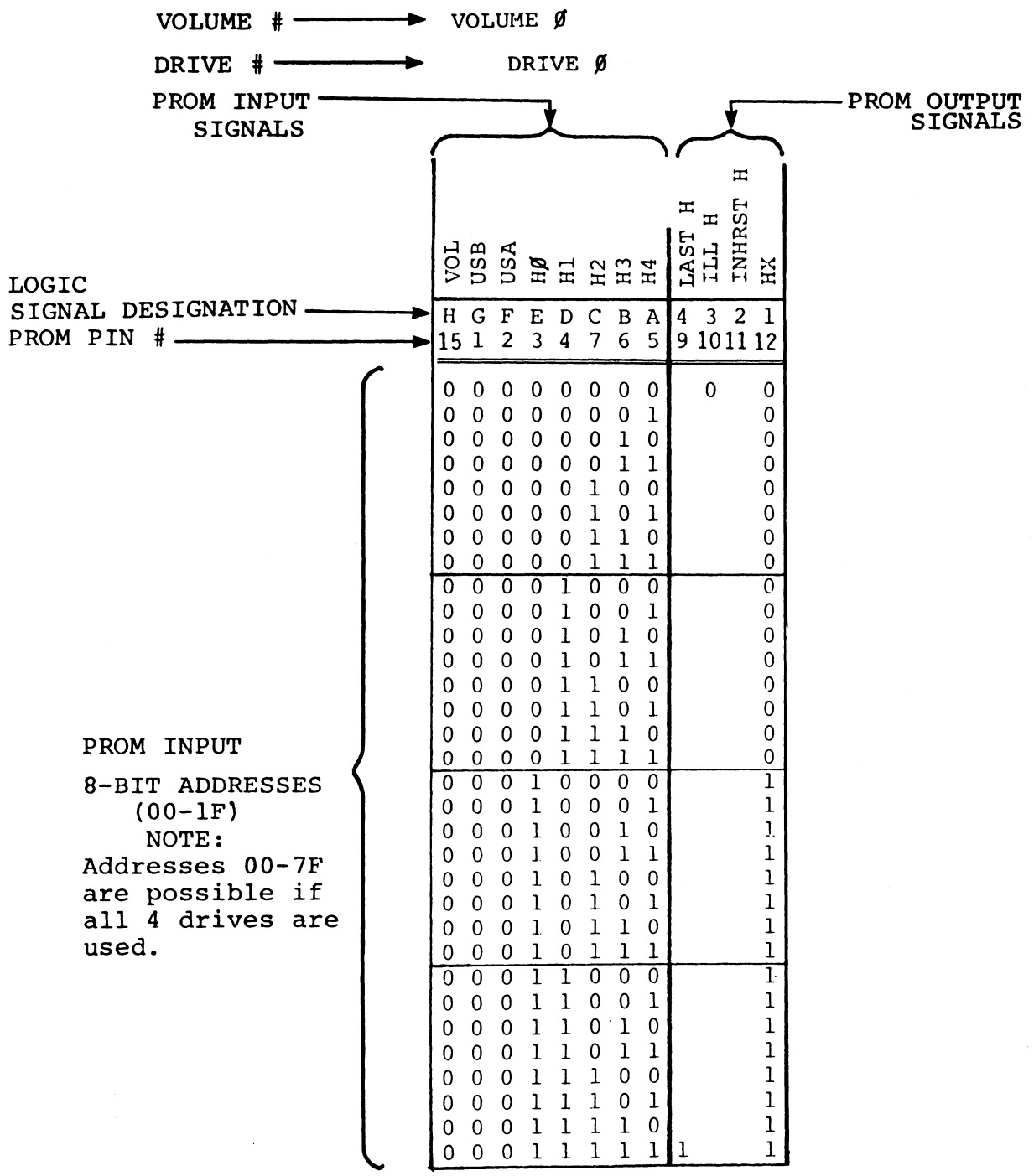
All LOTUS 700 Disc Controllers ordered from POINT 4 Data will require submission of Head PROM and Sector PROM Configuration Charts for the system configuration in which the controller is to be used. POINT 4 Data will program the Head and Sector PROMs according to these configuration charts.

The following two sections are provided for LOTUS 700 users who find it necessary to reconfigure a system after receipt of the 700 Controller board. Instructions for coding the information necessary to program the PROMs are provided. Appendix B contains examples of charts coded for specific disc drives.

2.5.1 Head PROM Configuration Chart Coding

The Head PROM Configuration Chart must be prepared to specify head information on each disc drive in the system.

The Head PROM Configuration Chart can be interpreted as follows:



VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX
H 15	G 1	F 2	E 3	D 4	C 7	B 6	A 5	4 9	3 10	2 11	1 12
0	0	0	0	0	0	0	0		0		0
0	0	0	0	0	0	0	1				0
0	0	0	0	0	0	1	0				0
0	0	0	0	0	0	1	1				0
0	0	0	0	0	1	0	0				0
0	0	0	0	0	1	0	1				0
0	0	0	0	0	1	1	0				0
0	0	0	0	0	1	1	1				0
0	0	0	0	1	0	0	0				0
0	0	0	0	1	0	0	1				0
0	0	0	0	1	0	1	0				0
0	0	0	0	1	0	1	1				0
0	0	0	0	1	1	0	0				0
0	0	0	0	1	1	0	1				0
0	0	0	0	1	1	1	0				0
0	0	0	0	1	1	1	1				0
0	0	0	1	0	0	0	0				1
0	0	0	1	0	0	0	1				1
0	0	0	1	0	0	1	0				1
0	0	0	1	0	0	1	1				1
0	0	0	1	0	1	0	0				1
0	0	0	1	0	1	0	1				1
0	0	0	1	0	1	1	0				1
0	0	0	1	0	1	1	1				1
0	0	0	1	1	0	0	0				1
0	0	0	1	1	0	0	1				1
0	0	0	1	1	0	1	0				1
0	0	0	1	1	0	1	1				1
0	0	0	1	1	1	0	0				1
0	0	0	1	1	1	0	1				1
0	0	0	1	1	1	1	0				1
0	0	0	1	1	1	1	1	1			1

A sample of a Head PROM Configuration Chart format can be found in Figure 2-3.

VOLUME Ø DRIVE Ø									LAST H	ILL H	INHRST H		DRIVE 1								LAST H	ILL H	INHRST H		DRIVE 2								LAST H	ILL H	INHRST H		74S287 DRIVE 3								22C LAST H	ILL H	INHRST H	
VOL	USB	USA	HØ	H1	H2	H3	H4					HX	VOL	USB	USA	HØ	H1	H2	H3	H4				HX	VOL	USB	USA	HØ	H1	H2	H3	H4				HX	VOL	USB	USA	HØ	H1	H2	H3	H4				HX
H	G	F	E	D	C	B	A		4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5		9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12
0	0	0	0	0	0	0	0			0		0	0	0	1	0	0	0	0	0		0		0	0	1	0	0	0	0	0	0		0		0	0	1	1	0	0	0	0		0		0
0	0	0	0	0	0	0	1					0	0	0	1	0	0	0	0	1				0	0	1	0	0	0	0	0	1				0	0	1	1	0	0	0	1				0
0	0	0	0	0	0	1	0					0	0	0	1	0	0	0	1	0				0	0	1	0	0	0	0	1	0				0	0	1	1	0	0	0	1	0			0
0	0	0	0	0	0	1	1					0	0	0	1	0	0	0	1	1				0	0	1	0	0	0	0	1	1				0	0	1	1	0	0	0	1	1			0
0	0	0	0	0	1	0	0					0	0	0	1	0	0	1	0	0				0	0	1	0	0	0	0	1	0	0			0	0	1	1	0	0	1	0	0			0
0	0	0	0	0	1	0	1					0	0	0	1	0	0	1	0	1				0	0	1	0	0	0	0	1	0	1			0	0	1	1	0	0	1	0	1			0
0	0	0	0	0	1	1	0					0	0	0	1	0	0	1	1	0				0	0	1	0	0	0	0	1	0	1	0		0	0	1	1	0	0	1	1	0			0
0	0	0	0	0	1	1	1					0	0	0	1	0	0	1	1	1				0	0	1	0	0	0	0	1	0	1	1		0	0	1	1	0	0	1	1	1			0
0	0	0	0	1	0	0	0					0	0	0	1	0	1	0	0	0				0	0	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1	0	0	0			0
0	0	0	0	1	0	0	1					0	0	0	1	0	1	0	0	1				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	0	1	0	1	0					0	0	0	1	0	1	0	1	0				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	0	1	0	1	1					0	0	0	1	0	1	0	1	1				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	0	1	1	0	0					0	0	0	1	0	1	1	0	0				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	0	1	1	0	1					0	0	0	1	0	1	1	0	1				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	0	1	1	1	0					0	0	0	1	0	1	1	1	0				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	0	1	1	1	1					0	0	0	1	0	1	1	1	1				0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1			0
0	0	0	1	0	0	0	0					1	0	0	1	1	0	0	0	0				1	0	1	0	1	0	0	0	0				1	0	1	1	1	0	0	0	0			1
0	0	0	1	0	0	0	1					1	0	0	1	1	0	0	0	1				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	0	0	1			1
0	0	0	1	0	0	1	0					1	0	0	1	1	0	0	1	0				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	0	1	0			1
0	0	0	1	0	0	1	1					1	0	0	1	1	0	0	1	1				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	0	1	1			1
0	0	0	1	0	1	0	0					1	0	0	1	1	0	1	0	0				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	1	0	0			1
0	0	0	1	0	1	0	1					1	0	0	1	1	0	1	0	1				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	1	0	1			1
0	0	0	1	0	1	1	0					1	0	0	1	1	0	1	1	0				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	1	1	0			1
0	0	0	1	0	1	1	1					1	0	0	1	1	0	1	1	1				1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	1	1	1			1
0	0	0	1	1	0	0	0					1	0	0	1	1	1	0	0	0				1	0	1	0	1	1	0	0	0				1	0	1	1	1	1	0	0	0			1
0	0	0	1	1	0	0	1					1	0	0	1	1	1	0	0	1				1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	0	0	1			1
0	0	0	1	1	0	1	0					1	0	0	1	1	1	0	1	0				1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	0	1	0			1
0	0	0	1	1	0	1	1					1	0	0	1	1	1	0	1	1				1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	0	1	1			1
0	0	0	1	1	1	0	0					1	0	0	1	1	1	1	0	0				1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	1	0	0			1
0	0	0	1	1	1	0	1					1	0	0	1	1	1	1	0	1				1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	1	0	1			1
0	0	0	1	1	1	1	0					1	0	0	1	1	1	1	1	0				1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	1	1	0			1
0	0	0	1	1	1	1	1		1			1	0	0	1	1	1	1	1	1	1			1	0	1	0	1	1	0	0	0	1			1	0	1	1	1	1	1	1	1	1		1

SH. 1.

Figure 2-3. Head PROM Configuration Chart (Sheet 1)

VOLUME 1 DRIVE Ø									LAST H	ILL H	INHRST H	HX	DRIVE 1												DRIVE 2												745287 DRIVE 3									22C			
VOL	USB	USA	HØ	H1	H2	H3	H4						VOL	USB	USA	HØ	H1	H2	H3	H4					VOL	USB	USA	HØ	H1	H2	H3	H4					VOL	USB	USA	HØ	H1	H2	H3	H4				
H15	G1	F2	E3	D4	C7	B6	A5		4 9	3 10	2 11	1 12	H15	G1	F2	E3	D4	C7	B6	A5	4 9	3 10	2 11	1 12	H15	G1	F2	E3	D4	C7	B6	A5	4 9	3 10	2 11	1 12	H15	G1	F2	E3	D4	C7	B6	A5	4 9	3 10	2 11	1 12
1	0	0	0	0	0	0	0					1	1	0	1	0	0	0	0	0				1	1	1	0	0	0	0	0	0				1	1	1	1	0	0	0	0				1
1	0	0	0	0	0	0	1					1	1	0	1	0	0	0	0	1				1	1	1	0	0	0	0	0	1				1	1	1	1	0	0	0	0	1			1
1	0	0	0	0	0	1	0					1	1	0	1	0	0	0	1	0				1	1	1	0	0	0	0	1	0				1	1	1	1	0	0	0	1	0			1
1	0	0	0	0	0	1	1					1	1	0	1	0	0	0	1	1				1	1	1	0	0	0	0	1	1				1	1	1	1	0	0	0	1	1			1
1	0	0	0	0	1	0	0					1	1	0	1	0	0	1	0	0				1	1	1	0	0	0	0	1	0	0			1	1	1	1	0	0	1	0	0			1
1	0	0	0	0	1	0	1					1	1	0	1	0	0	1	0	1				1	1	1	0	0	0	0	1	0	1			1	1	1	1	0	0	1	0	1			1
1	0	0	0	0	1	1	0					1	1	0	1	0	0	1	1	0				1	1	1	0	0	0	0	1	1	0			1	1	1	1	0	0	1	1	0			1
1	0	0	0	0	1	1	1					1	1	0	1	0	0	1	1	1				1	1	1	0	0	0	0	1	1	1			1	1	1	1	0	0	1	1	1			1
1	0	0	0	1	0	0	0					1	1	0	1	0	1	0	0	0				1	1	1	0	0	0	0	1	0	0	0		1	1	1	1	0	1	0	0	0			1
1	0	0	0	1	0	0	1					1	1	0	1	0	1	0	0	1				1	1	1	0	0	0	0	1	0	0	1		1	1	1	1	0	1	0	0	1			1
1	0	0	0	1	0	1	0					1	1	0	1	0	1	0	1	0				1	1	1	0	0	0	0	1	0	1	0		1	1	1	1	0	1	0	1	0			1
1	0	0	0	1	0	1	1					1	1	0	1	0	1	0	1	1				1	1	1	0	0	0	0	1	0	1	1		1	1	1	1	0	1	0	1	1			1
1	0	0	0	1	1	0	0					1	1	0	1	0	1	1	0	0				1	1	1	0	0	0	0	1	1	0	0		1	1	1	1	0	1	1	0	0			1
1	0	0	0	1	1	0	1					1	1	0	1	0	1	1	0	1				1	1	1	0	0	0	0	1	1	0	1		1	1	1	1	0	1	1	0	1			1
1	0	0	0	1	1	1	0					1	1	0	1	0	1	1	1	0				1	1	1	0	0	0	0	1	1	1	0		1	1	1	1	0	1	1	1	0			1
1	0	0	0	1	1	1	1					1	1	0	1	0	1	1	1	1				1	1	1	0	0	0	0	1	1	1	1		1	1	1	1	0	1	1	1	1			1
1	0	0	1	0	0	0	0		1	1	0	1	1	0	1	1	0	0	0	0	1	1	0	1	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	1
1	0	0	1	0	0	0	1		1	1	0	1	1	0	1	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	1	1	1	1	0	0	0	1	1	1	0	1
1	0	0	1	0	0	1	0		1	1	0	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1
1	0	0	1	0	0	1	1		1	1	0	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	1	1	1	1	0	0	1	1	1	1	0	1
1	0	0	1	0	1	0	0		1	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1	1	1	0	1	0	0	0	1	0	0	0	1	1	1	1	1	0	1	0	0	1	1	0	1
1	0	0	1	0	1	0	1		1	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1	1	1	0	1	0	0	0	1	0	1	0	1	1	1	1	1	0	1	0	1	1	1	0	1
1	0	0	1	0	1	1	0		1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	1	0	1	0	0	0	1	0	1	1	0	1	1	1	1	0	1	1	0	1	1	0	1
1	0	0	1	0	1	1	1		1	1	0	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1	0	1	0	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	0	1
1	0	0	1	1	0	0	0		1	1	0	1	1	0	1	1	1	0	0	0	1	1	0	1	1	1	0	1	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	1	1	0	1
1	0	0	1	1	0	0	1		1	1	0	1	1	0	1	1	1	0	0	1	1	1	0	1	1	1	0	1	1	0	0	0	1	1	1	0	1	1	1	1	1	0	0	1	1	1	0	1
1	0	0	1	1	0	1	0		1	1	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	1	0	1	1	0	0	0	1	0	1	0	1	1	1	1	1	0	1	0	1	1	0	1
1	0	0	1	1	0	1	1		1	1	0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0	0	0	1	0	1	1	1	1	1	1	1	0	1	1	1	1	0	1
1	0	0	1	1	1	0	0		1	1	0	1	1	0	1	1	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	1	0	0	1	1	0	1
1	0	0	1	1	1	0	1		1	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	0	1
1	0	0	1	1	1	1	0		1	1	0	1	1	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1	0	0	0	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1
1	0	0	1	1	1	1	1		1	1	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1

SH. 2.

Figure 2-3. Head PROM Configuration Chart (Sheet 2)

Input signals for Head PROM addressing are:

Volume #	VOL
Drive #	USB, USA
Head #	H0, H1, H2, H3, H4

Output signals generated by the Head PROM are:

LAST H	1 indicates the last head (surface) in this volume
ILL H	1 indicates an illegal head (surface) for this volume
INHRST H	0 indicates normal organization 1 indicates horizontal organization
Hx	Hx = 0 for Volume 0 Hx = 1 for Volume 1

To program the Head PROM use the following procedure:

1. Determine the type of drives to be used as Drive 0, 1, 2, and 3.

2. Determine the number of logical heads in each drive.

3. Prepare a Head PROM Configuration Chart as shown in Figure 2-3. To fill in the PROM output signal information, use the following guidelines:

   Hx = H0 + VOL

ILL H = 0	For valid head number
= 1	For illegal head number
LAST H = 1	For last head or illegal head numbers
INHRST H = 0	For normal operation
= 1	For horizontal organization in multi-surface volumes

   (NOTE: If INHRST H = 1, make LAST H = 1 also)

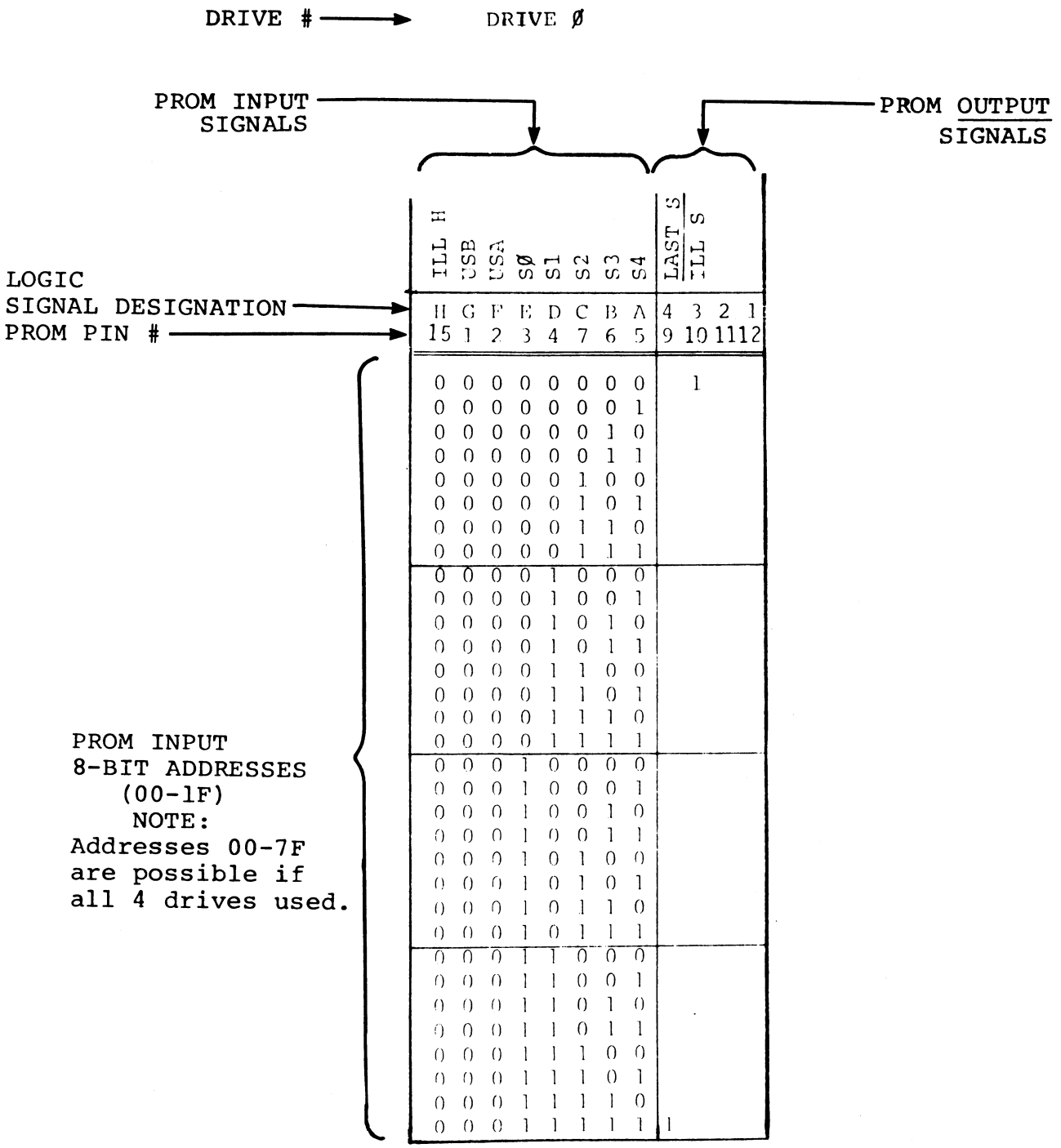
   The above information must be filled in for each volume (sheets 1 and 2 of the Head PROM Configuration Chart.

4. Having properly coded the Head PROM Configuration sheets. The user can program Head PROMs using the chart as program input to the PROM. The PROM I.C. required is a 74S287 and the P.C. board location for installation of the PROM is 22C. installation of the PROM is 22C.

2.5.2 Sector PROM Configuration Chart Coding

The Sector PROM Configuration Chart must be prepared to specify sector information on each disc drive in the system.

The Sector PROM Configuration Chart can be interpreted as follows:



A sample of a Sector PROM Configuration Chart format can be found in Figure 2-4.

DRIVE Ø										DRIVE 1										DRIVE 2										74S287 DRIVE 3										19C
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S		ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S		ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S		ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S	
H	G	F	E	D	C	B	A	4	3 2 1	H	G	F	E	D	C	B	A	4	3 2 1	H	G	F	E	D	C	B	A	4	3 2 1	H	G	F	E	D	C	B	A	4	3 2 1
15	1	2	3	4	7	6	5	9	10 11 12	15	1	2	3	4	7	6	5	9	10 11 12	15	1	2	3	4	7	6	5	9	10 11 12	15	1	2	3	4	7	6	5	9	10 11 12
0	0	0	0	0	0	0	0	1		0	0	1	0	0	0	0	0	1		0	1	0	0	0	0	0	0	1		0	1	1	0	0	0	0	0	1	
0	0	0	0	0	0	0	1			0	0	1	0	0	0	0	1			0	1	0	0	0	0	0	1			0	1	1	0	0	0	0	1		
0	0	0	0	0	0	1	0			0	0	1	0	0	0	1	0			0	1	0	0	0	0	1	0			0	1	1	0	0	0	1	0		
0	0	0	0	0	0	1	1			0	0	1	0	0	0	1	1			0	1	0	0	0	0	1	1			0	1	1	0	0	0	1	1		
0	0	0	0	0	1	0	0			0	0	1	0	0	1	0	0			0	1	0	0	0	1	0	0			0	1	1	0	0	1	0	0		
0	0	0	0	0	1	0	1			0	0	1	0	0	1	0	1			0	1	0	0	0	1	0	1			0	1	1	0	0	1	0	1		
0	0	0	0	0	1	1	0			0	0	1	0	0	1	1	0			0	1	0	0	0	1	1	0			0	1	1	0	0	1	1	0		
0	0	0	0	0	1	1	1			0	0	1	0	0	1	1	1			0	1	0	0	0	1	1	1			0	1	1	0	0	1	1	1		
0	0	0	0	1	0	0	0			0	0	1	0	1	0	0	0			0	1	0	0	1	0	0	0			0	1	1	0	1	0	0	0		
0	0	0	0	1	0	0	1			0	0	1	0	1	0	0	1			0	1	0	0	1	0	0	1			0	1	1	0	1	0	0	1		
0	0	0	0	1	0	1	0			0	0	1	0	1	0	1	0			0	1	0	0	1	0	1	0			0	1	1	0	1	0	1	0		
0	0	0	0	1	0	1	1			0	0	1	0	1	0	1	1			0	1	0	0	1	0	1	1			0	1	1	0	1	0	1	1		
0	0	0	0	1	1	0	0			0	0	1	0	1	1	0	0			0	1	0	0	1	1	0	0			0	1	1	0	1	1	0	0		
0	0	0	0	1	1	0	1			0	0	1	0	1	1	0	1			0	1	0	0	1	1	0	1			0	1	1	0	1	1	0	1		
0	0	0	0	1	1	1	0			0	0	1	0	1	1	1	0			0	1	0	0	1	1	1	0			0	1	1	0	1	1	1	0		
0	0	0	0	1	1	1	1			0	0	1	0	1	1	1	1			0	1	0	0	1	1	1	1			0	1	1	0	1	1	1	1		
0	0	0	1	0	0	0	0			0	0	1	1	0	0	0	0			0	1	0	1	0	0	0	0			0	1	1	1	0	0	0	0		
0	0	0	1	0	0	0	1			0	0	1	1	0	0	0	1			0	1	0	1	0	0	0	1			0	1	1	1	0	0	0	1		
0	0	0	1	0	0	1	0			0	0	1	1	0	0	1	0			0	1	0	1	0	0	1	0			0	1	1	1	0	0	1	0		
0	0	0	1	0	0	1	1			0	0	1	1	0	0	1	1			0	1	0	1	0	0	1	1			0	1	1	1	0	0	1	1		
0	0	0	1	0	1	0	0			0	0	1	1	0	1	0	0			0	1	0	1	0	1	0	0			0	1	1	1	0	1	0	0		
0	0	0	1	0	1	0	1			0	0	1	1	0	1	0	1			0	1	0	1	0	1	0	1			0	1	1	1	0	1	0	1		
0	0	0	1	0	1	1	0			0	0	1	1	0	1	1	0			0	1	0	1	0	1	1	0			0	1	1	1	0	1	1	0		
0	0	0	1	0	1	1	1			0	0	1	1	0	1	1	1			0	1	0	1	0	1	1	1			0	1	1	1	0	1	1	1		
0	0	0	1	1	0	0	0			0	0	1	1	1	0	0	0			0	1	0	1	1	0	0	0			0	1	1	1	1	0	0	0		
0	0	0	1	1	0	0	1			0	0	1	1	1	0	0	1			0	1	0	1	1	0	0	1			0	1	1	1	1	0	0	1		
0	0	0	1	1	0	1	0			0	0	1	1	1	0	1	0			0	1	0	1	1	0	1	0			0	1	1	1	1	0	1	0		
0	0	0	1	1	0	1	1			0	0	1	1	1	0	1	1			0	1	0	1	1	0	1	1			0	1	1	1	1	0	1	1		
0	0	0	1	1	1	0	0			0	0	1	1	1	1	0	0			0	1	0	1	1	1	0	0			0	1	1	1	1	1	0	0		
0	0	0	1	1	1	0	1			0	0	1	1	1	1	0	1			0	1	0	1	1	1	0	1			0	1	1	1	1	1	0	1		
0	0	0	1	1	1	1	0			0	0	1	1	1	1	1	0			0	1	0	1	1	1	1	0			0	1	1	1	1	1	1	0		
0	0	0	1	1	1	1	1	1		0	0	1	1	1	1	1	1	1		0	1	0	1	1	1	1	1	1		0	1	1	1	1	1	1	1		1

SH. 1.

Figure 2-4. Sector PROM Configuration Chart (Sheet 1)

DRIVE Ø																DRIVE 1															
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S								ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S							
H 15	G 1	F 2	E 3	D 4	C 7	B 6	A 5	4 9	3 10	2 11	1 12					H 15	G 1	F 2	E 3	D 4	C 7	B 6	A 5	4 9	3 10	2 11	1 12				
1	0	0	0	0	0	0	0	1	0							1	0	1	0	0	0	0	0	1	0						
1	0	0	0	0	0	0	1	1	0							1	0	1	0	0	0	0	1	1	0						
1	0	0	0	0	0	1	0	1	0							1	0	1	0	0	0	1	0	1	0						
1	0	0	0	0	0	1	1	1	0							1	0	1	0	0	0	1	1	1	0						
1	0	0	0	0	1	0	0	1	0							1	0	1	0	0	1	0	0	1	0						
1	0	0	0	0	1	0	1	1	0							1	0	1	0	0	1	0	1	1	0						
1	0	0	0	0	1	1	0	1	0							1	0	1	0	0	1	1	0	1	0						
1	0	0	0	0	1	1	1	1	0							1	0	1	0	0	1	1	1	1	0						
1	0	0	0	1	0	0	0	1	0							1	0	1	0	1	0	0	0	1	0						
1	0	0	0	1	0	0	1	1	0							1	0	1	0	1	0	0	1	1	0						
1	0	0	0	1	0	1	0	1	0							1	0	1	0	1	0	1	0	1	0						
1	0	0	0	1	0	1	1	1	0							1	0	1	0	1	0	1	1	1	0						
1	0	0	0	1	1	0	0	1	0							1	0	1	0	1	1	0	0	1	0						
1	0	0	0	1	1	0	1	1	0							1	0	1	0	1	1	0	1	1	0						
1	0	0	0	1	1	1	0	1	0							1	0	1	0	1	1	1	0	1	0						
1	0	0	0	1	1	1	1	1	0							1	0	1	0	1	1	1	1	1	0						
1	0	0	1	0	0	0	0	1	0							1	0	1	1	0	0	0	0	1	0						
1	0	0	1	0	0	0	1	1	0							1	0	1	1	0	0	0	1	1	0						
1	0	0	1	0	0	1	0	1	0							1	0	1	1	0	0	1	0	1	0						
1	0	0	1	0	0	1	1	1	0							1	0	1	1	0	0	1	1	1	0						
1	0	0	1	0	1	0	0	1	0							1	0	1	1	0	1	0	0	1	0						
1	0	0	1	0	1	0	1	1	0							1	0	1	1	0	1	0	1	1	0						
1	0	0	1	0	1	1	0	1	0							1	0	1	1	0	1	1	0	1	0						
1	0	0	1	0	1	1	1	1	0							1	0	1	1	0	1	1	1	1	0						
1	0	0	1	1	0	0	0	1	0							1	0	1	1	1	0	0	0	1	0						
1	0	0	1	1	0	0	1	1	0							1	0	1	1	1	0	0	1	1	0						
1	0	0	1	1	0	1	0	1	0							1	0	1	1	1	0	1	0	1	0						
1	0	0	1	1	0	1	1	1	0							1	0	1	1	1	0	1	1	1	0						
1	0	0	1	1	1	0	0	1	0							1	0	1	1	1	1	0	0	1	0						
1	0	0	1	1	1	0	1	1	0							1	0	1	1	1	1	0	1	1	0						
1	0	0	1	1	1	1	0	1	0							1	0	1	1	1	1	1	0	1	0						
1	0	0	1	1	1	1	1	1	0							1	0	1	1	1	1	1	1	1	0						

DRIVE 2																74S287 DRIVE 3																19C
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S								ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S / ILL S								
H 15	G 1	F 2	E 3	D 4	C 7	B 6	A 5	4 9	3 10	2 11	1 12					H 15	G 1	F 2	E 3	D 4	C 7	B 6	A 5	4 9	3 10	2 11	1 12					
1	1	0	0	0	0	0	0	1	0							1	1	1	0	0	0	0	0	1	0							
1	1	0	0	0	0	0	1	1	0							1	1	1	0	0	0	0	1	1	0							
1	1	0	0	0	0	1	0	1	0							1	1	1	0	0	0	1	0	1	0							
1	1	0	0	0	0	1	1	1	0							1	1	1	0	0	0	1	1	1	0							
1	1	0	0	0	1	0	0	1	0							1	1	1	0	0	1	0	0	1	0							
1	1	0	0	0	1	0	1	1	0							1	1	1	0	0	1	0	1	1	0							
1	1	0	0	0	1	1	0	1	0							1	1	1	0	0	1	1	0	1	0							
1	1	0	0	0	1	1	1	1	0							1	1	1	0	0	1	1	1	1	0							
1	1	0	0	1	0	0	0	1	0							1	1	1	0	1	0	0	0	1	0							
1	1	0	0	1	0	0	1	1	0							1	1	1	0	1	0	0	1	1	0							
1	1	0	0	1	0	1	0	1	0							1	1	1	0	1	0	1	0	1	0							
1	1	0	0	1	0	1	1	1	0							1	1	1	0	1	0	1	1	1	0							
1	1	0	0	1	1	0	0	1	0							1	1	1	0	1	1	0	0	1	0							
1	1	0	0	1	1	0	1	1	0							1	1	1	0	1	1	0	1	1	0							
1	1	0	0	1	1	1	0	1	0							1	1	1	0	1	1	1	0	1	0							
1	1	0	0	1	1	1	1	1	0							1	1	1	0	1	1	1	1	1	0							
1	1	0	1	0	0	0	0	1	0							1	1	1	1	0	0	0	0	1	0							
1	1	0	1	0	0	0	1	1	0							1	1	1	1	0	0	0	1	1	0							
1	1	0	1	0	0	1	0	1	0							1	1	1	1	0	0	1	0	1	0							
1	1	0	1	0	0	1	1	1	0							1	1	1	1	0	0	1	1	1	0							
1	1	0	1	0	1	0	0	1	0							1	1	1	1	0	1	0	0	1	0							
1	1	0	1	0	1	0	1	1	0							1	1	1	1	0	1	0	1	1	0							
1	1	0	1	0	1	1	0	1	0							1	1	1	1	0	1	1	0	1	0							
1	1	0	1	0	1	1	1	1	0							1	1	1	1	0	1	1	1	1	0							
1	1	0	1	1	0	0	0	1	0							1	1	1	1	1	0	0	0	1	0							
1	1	0	1	1	0	0	1	1	0							1	1	1	1	1	0	0	1	1	0							
1	1	0	1	1	0	1	0	1	0							1	1	1	1	1	0	1	0	1	0							
1	1	0	1	1	0	1	1	1	0							1	1	1	1	1	0	1	1	1	0							
1	1	0	1	1	1	0	0	1	0							1	1	1	1	1	1	0	0	1	0							
1	1	0	1	1	1	0	1	1	0							1	1	1	1	1	1	0	1	1	0							
1	1	0	1	1	1	1	0	1	0							1	1	1	1	1	1	1	0	1	0							
1	1	0	1	1	1	1	1	1	0							1	1	1	1	1	1	1	1	1	0							

SH. 2.

Figure 2-4. Sector PROM Configuration Chart (Sheet 2)

Input signals for Sector PROM addressing are:

Illegal Head	ILL H
Drive #	USB, USA
Sector #	S0, S1, S2, S3, S4

Output signals generated by the Sector PROM are:

LAST S	1 indicates the last sector on any track
ILL S	1 indicates that the sector # exceeds the capacity of the drive, or indicates that ILL H is set to 1

To program the Sector PROM use the following procedure:

1. Determine the type of drives to be used as Drive 0, 1, 2, and 3.

2. Determine the number of sectors per track for each drive.

3. Prepare a Sector PROM Configuration Chart as shown in Figure 2-4. To fill in the PROM output signal information, use the following guidelines:

LAST S = 1	For last sector or ILL H = 1
ILL S = 0	For illegal sector number or for ILL H = 1

4. Verify that sector count in each drive matches that coded in the Sector PROM Configuration Chart.

5. Having properly coded the Sector PROM Configuration sheets, the user can program Sector PROMs using the charts as program input to the PROM. The PROM I.C. required is a 74S287 and the P.C. board location for installation of the PROM is 19C.

Section 3
PROGRAMMING

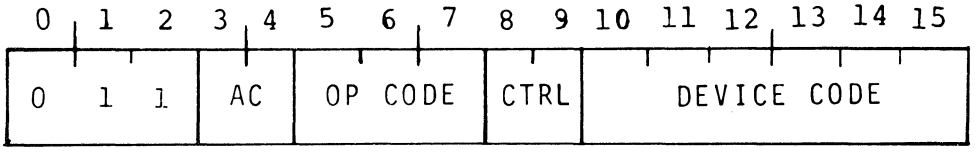
3.1 INTRODUCTION

This section outlines the programming protocols for driving up to four storage module-type drives via POINT 4 Data's Lotus 700 Disc Controller. Covered are: instructions for programming data channel transfers, disc controller commands, error conditions and flags, disc formatting and error correction procedures.

3.2 INSTRUCTIONS

Input/Output Instructions enable the processor to communicate with peripheral devices in the computer system. I/O instructions transfer data between accumulators and devices or device controllers, start or reset device operation, and check the status of each device. These instructions also transfer information on the starting block in computer memory, the block length, the disc cylinder/surface/starting sector address and the function to be performed. Each I/O instruction contains a 6-bit device code field that specifies the particular device for this data transfer.

All I/O instruction words have the following format:



An I/O instruction is designated by 011 in bits 0-2. The OPCODE and Control (CTRL) fields define the I/O operation to be performed. When a register data transfer is involved, the AC field (bits 3-4) specifies the accumulator involved in the data transfer. Bits 10-15 select the device that is to respond to the instruction.

In order to program register data transfers, the programmer must properly code the processor instruction and also load the specified processor accumulator (if required) with the information to be transferred to the controller. Data-out (to the controller) transfers require both the instruction coding and loading of an accumulator with information for the disc

controller. Data-in (to the processor) transfers require only instruction coding since information will be read from the disc controller into the specified accumulator.

Four data-out instructions supply the controller with all information necessary to perform any operation required. To obtain status information from the controller, seven data-in instructions are provided.

In the description that follows, coding conventions are used so that the assembler can recognize and translate the instruction into machine language. Instructions are coded according to the following format.

MNEMONIC [optional mnemonics] **OPERAND STRING**

The mnemonic shown in BOLD must be coded exactly as shown in the instruction description. For example, the mnemonic for the "data-out to buffer A" instruction is:

DOA

Operands printed in BOLD are also required to be coded exactly as shown.

Some instructions have optional mnemonics that are appended to the main mnemonic if the option is desired. These mnemonics are enclosed in [ ]. Optional mnemonics may require substitution of a specific control character in order to be properly decoded. Instructions for controlling data transfer between the processor and the disc subsystem use two optional fields:

ac = Accumulator
f = Control Function Flag

The accumulator field (ac) specifies the accumulator number from which information is to be gained or into which information will be loaded during the data transfer.

The control function field controls the disc controller's BUSY and DONE flags as follows:

f = S (start)	Sets BUSY flag to one (1); clears DONE flag to zero (0); clears all controller error flags; starts R/W timeout. Disables drive attention interrupts; starts the following operations as specified in the command: read, read offset, format, write header, verify, read buffer, write, read header.

f = C (Clear)	Clears BUSY flag to zero (0); clears DONE flag to zero (0); terminates any data transfer operation; clears all controller error flags; clears all drive attention flags. It does not terminate seek or recalibrate commands.
f = P (Pulse)	Sets the control-full flag to one (1) and starts the following operations as specified in the command: recalibrate, seek release, trespass.

A special instruction is used to initialize and clear all flags in all I/O devices. This instruction, IORST, performs the following functions in the disc controller:

Performs all operations listed above at f = C; initiates a recalibrate operation on the lowest numbered ready/non-reserved drive. Sets the surface/sector address register to zero, sets the command register to zero, sets the memory address register to zero.

3.2.1 Specify Command and Drive Instruction

Instruction Mnemonic: **DOA**[f] ac,**DSKP**

Instruction Function: Clears the DONE/DRIVE ATTENTION flags, as selected by bits 0-4 of the specified AC, to zero (0). Loads bits 5-8 of the AC into the controller's command register. Loads bits 9 and 10 of the AC into the controller's drive select register. For CMD drives, loads bit 11 into the controller's volume select register. Loads bits 12-15 into the auxiliary register.

NOTE

This instruction is ignored if the control-full bit is set to one (1).

Accumulator Format:

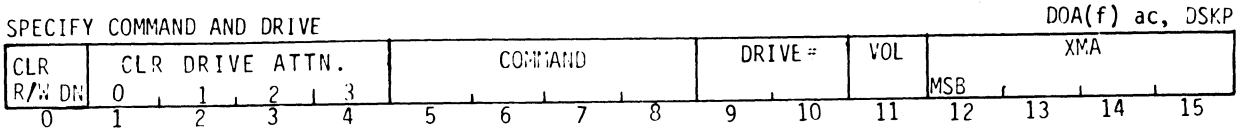


Chart of Accumulator Bit Functions:

Bits	Functions
0	Clears R/W DONE flag.
1-4	Clears the respective Seek DONE/ATTENTION flags for drives 0-3
5-8	Command: 0000 Read 0001 Recalibrate 0010 Seek 0011 Write header 0100 Read offset + 0101 Read offset - 0110 Format 0111 Release 1000 Trespass 1001 Alternate Mode 1 1010 Alternate Mode 2 1011 No operation 1100 Verify 1101 Read FIFO buffer 1110 Write 1111 Read format
9-10	Selects drive. Also selects drive status register.
11	Volume select bit. Defines non-removeable surface(s) in CMD drives.
12-15	Extended memory address (optional).

3.2.1.1 Detailed Description of Commands

Accumulator bits 5-8 transferred by the DOA instruction call for a command to be given to the controller. The 16 possible commands cause the controller to interact with the specified drive and perform the function indicated in the command. The chart below gives detailed descriptions of the controller and disc drive operations which result from each of the 16 commands.

Command Name	Bit Config.	Resulting Operations
READ	0000	Reads data up to 32 consecutive sectors from the selected drive starting at the specified surface and sector on the cylinder selected by the previous seek command. Data is read from up to 32 consecutive sectors into computer memory starting at the specified memory address. Surface or cylinder boundaries are crossed if necessary. The controller finds and verifies the header of the desired sector(s); reads the data and transmits it via the DMA channel to computer memory. During sector read the controller accumulates an ECC checkword. The ECC checkword is compared with the checkword recorded in the ECC words recorded when the data was written to disc. If an ECC error is detected, the same sector is reread and retransmitted. If an ECC error occurs again, the operation is terminated.
RECALIBRATE	0001	Moves the heads of the selected disc drive to cylinder zero (0) and attempts to clear drive faults (if any).
SEEK	0010	Moves the heads of the selected disc drive to the specified cylinder. In cartridge module drives, switches to the desired volume.

Command Name	Bit Config.	Resulting Operations
WRITE HEADER	0011	Writes the three header words, transferred from the specified computer memory address, into up to 32 consecutive sectors in the selected drive. Data is written from memory starting at the specified memory address onto the disc starting at the specified surface and sector on the cylinder selected by the previous seek command. Surface or cylinder boundaries are crossed if necessary. The controller finds the specified sector and writes the preamble, sink bit, header, header CRC, and gap into the sector using the three words from memory. Any data previously written in this sector remains intact.
READ OFFSET +	0100	Same as a Read command except with the disc drive heads offset towards the spindle. This command is used for data recovery. Offset is only for the duration of this command.
READ OFFSET -	0101	Same as a Read command except with the disc drive heads offset away from the spindle. This command is used for data recovery. Offset is only for the duration of this command.
FORMAT	0110	Formats up to 32 consecutive sectors in the selected disc drive starting at the specified surface and sector on the cylinder selected by the previous seek command. Surface or cylinder boundaries are crossed if necessary. The controller finds the specified sector and writes the preamble, sink bit, header, header CRC, gap, data splice/preamble, sink bit, all zero data, ECC and postamble into the sector using address information from the controller. Any data previously written in this sector is lost.

Command Name	Bit Config.	Resulting Operations
RELEASE DRIVE	0111	Clears the reserved status of the drive selected in the DOA instruction. Clearing reserved status applies only to this status in relation to the processor issuing a DOA instruction (Dual Processor System).
TRESPASS	1000	Clears the reserved status of the drive selected in the DOA instruction, as reserved by the other processor in the system. It then reserves the selected drive for the processor issuing the DOA instruction (Dual Processor System).
ALTERNATE MODE 1	1001	In Alternate Mode 1, the DIA instruction reads the controller's memory address register and the DIB instruction reads the controller's extended memory address register.
ALTERNATE MODE 2	1010	In Alternate Mode 2, the DIA and DIB instructions read the ECC remainder words.
NO OPERATION	1011	None.
DATA VERIFY	1100	Reads up to 32 consecutive sectors from the selected drive, starting at the specified surface and sector on the cylinder selected by the previous seek command. Data read from the disc drive is compared word-by-word to data read from computer memory starting at the specified memory address. Surface or cylinder boundaries are crossed if necessary. The controller finds and verifies the header of the specified sector(s); reads the data and compares it to data read from computer memory. During sector read the controller accumulates an ECC checkword. This ECC checkword is compared with the recorded checkword. If an ECC or data compare error is detected, the operation terminates without retry.

Command Name	Bit Config.	Resulting Operations
READ FIFO	1101	This is a diagnostic test command. Eighteen words of data will be read into memory starting at the specified memory address. In order to read from the controller's FIFO into computer memory, the FIFO buffer must first be filled by issuing a write command to a write disabled drive.
WRITE	1110	Writes up to 32 consecutive sectors from memory starting at the specified memory address onto the selected drive. Writing starts at the specified surface and sector on the cylinder specified in the previous seek command. Surface or cylinder boundaries are crossed if necessary. The controller finds and verifies the header of the specified sector and writes 256 words of data from memory onto the specified sector. During write the controller accumulates a 32-bit ECC and appends it to the data field.
READ FORMAT	1111	The controller finds the desired sector and reads the three-word sector header, header CRC and two-word ECC from up to 32 consecutive sectors on the selected drive, starting at the specified surface and sector on the cylinder selected by the previous seek command. The data read is transferred into computer memory starting at the specified memory address. Surface or cylinder boundaries are crossed if necessary.

3.2.2 Specify Memory Address Instruction

Instruction Mnemonic: **DOB[f] ac,DSKP**

Instruction Function: Loads bits 0-15 of the specified AC into the controller's memory address register. Transfers the four XMA bits from the auxiliary register of the controller into the optional extended memory address register.

NOTE
This instruction is ignored if the BUSY flag is set to one (1).

Accumulator Format:

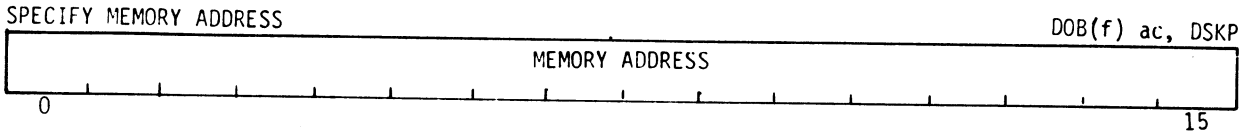


Chart of Accumulator Bit Functions:

Bits	Functions
0-15	Memory address of next data channel transfer.

3.2.3 Specify Cylinder Instruction

Instruction Mnemonic: **DOC**[f] ac,**DSKP**

(If the previous DOA specified a seek command)

Instruction Function: Loads bits 6-15 into the cylinder bits of the controller's cylinder register.

NOTE
This instruction is ignored if the control-full bit is set to one (1).

Accumulator Format:

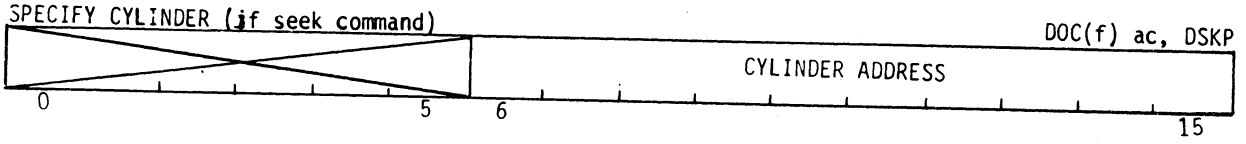


Chart of Accumulator Bit Functions:

Bits	Functions
0-5	Unused
6-15	Cylinder address for seek operation

3.2.4 Specify Surface, Sector and Sector Count Instruction

Instruction Mnemonic: **DOC**[f] ac,**DSKP**
(If the previous DOA specified other than a seek command)

Instruction Function: Loads bits 1-5 of the specified AC into the controller's surface address register. Loads bits 6-10 of the specified AC into the controller's sector address register. Loads bits 11-15 of the specified AC into the controller's sector count register.

NOTE
This instruction is ignored if the BUSY flag is set to one (1).

Accumulator Format:

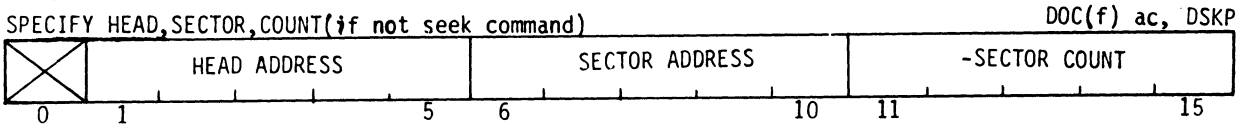


Chart of Accumulator Bit Functions:

Bits	Function
0	Unused.
1-5	Starting surface address for data transfer operation.
6-10	Starting sector address for data transfer operation.
11-15	Two's complement of the number of sectors to be transferred in one operation.

3.2.5 Read Controller Status Instruction

Instruction Mnemonic: **DIA[f] ac,DSKP**

Instruction Function: Loads the controller's status flags into bits 0-15 of the specified AC.

Accumulator Format:

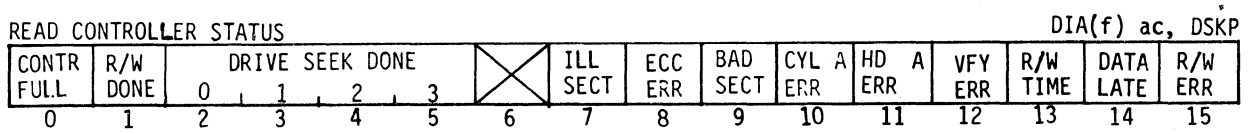


Chart of Accumulator Bit Functions:

Bits	Function
0	Control full. Drive command initiated by previous IOPLS has not yet been issued to the selected drive.
1	DONE flag of controller.
2-5	Seek DONE flags of drives. Respective drives have executed a recalibrate or seek command, became ready, or rejected an illegal seek command.
6	Unused.
7	Illegal sector/surface address.
8	ECC error during read or verify.
9	Bad sector flag was detected in desired sector header.
10	Cylinder address error was detected during sector header check.
11	Surface address error was detected during sector header check.
12	Verify error. Data read from disc did not match data read from memory.
13	R/W timeout. The data transfer operation was not completed in 1 second.
14	Data-late error. The FIFO buffer overflowed or underflowed during data transfer.
15	Controller error flag. One or more of bits 7 thru 14 is set to one (1), or a drive fault occurred on the drive selected for the current data transfer operation.

3.2.5.1 Controller Error Conditions

Accumulator bits 7-15 which are transferred to the computer by the DIA instruction carry controller status information to the processor. The accumulator bits and the error conditions flagged by setting of these bits to one (1) are listed below.

Accumulator Bit	Error Flag	Error Condition Description
7	ILLEGAL SECTOR/ SURFACE ADDRESS	The sector or surface address received by the controller for a data transfer operation exceeds the drive capacity set in the controller. Illegal sector/surface address is detected before any data transfer takes place. Operation terminates with the error flag and device-done flag set.
8	ECC ERROR	An ECC error has been detected during read or verify operations. An ECC error will cause one retry (read only). If the ECC error persists, operation terminates at the end of the sector with error flag and device-done flag set. The surface/sector address/sector count points to the next sector to be read.
9	BAD SECTOR	The bad sector flag is set in the header of the faulty sector. This sector cannot store data reliability. Data transfer is terminated promptly. The surface/sector address/sector count points to the sector in which the error occurred.
10	CYLINDER ADDRESS ERROR	The heads are not positioned on the cylinder specified by the previous seek operation. Data transfer operations are terminated promptly. The surface/sector address/sector count points to the sector in which the error occurred. A recalibrate command should be issued to the drive.

Accumulator Bit	Error Flag	Error Condition Description
11	SURFACE ADDRESS ERROR	Surface address in the sector header is different from the surface address currently specified. Data transfer operation is terminated promptly. The surface/sector address/sector count points to the sector in which the error occurred.
12	VERIFY ERROR	The data read from the disc did not match data read from computer memory. The data transfer operation is terminated at the end of the sector with error flags and device-done flags set to one (1). The surface/sector address/count points to the next sector to be verified.
13	READ/WRITE TIMEOUT	The data transfer operation initiated by the last "f = S (start)" was not completed in 1 second. The data transfer operation is terminated promptly. The surface/sector address/sector count points to the sector in which the error occurred.
14	DATA LATE ERROR	The FIFO buffer overflowed or underflowed. The data channel did not support the transfer rate required by the controller. Data transfer operation is terminated promptly. The surface/sector address/sector count points to the sector in which the error occurred.
15	CONTROLLER ERROR FLAG	One or more error flags listed above or a drive error flag (see subsection 3.2.6.1) on the drive selected has been set to one (1).

3.2.6 Read Drive Status Instruction

Instruction Mnemonic: **DIB[f] ac,DSKP**

Instruction Function: Loads the drive status flags of the drive selected by the previous DOA instruction into bits 0-15 of the specified AC.

Accumulator Format:

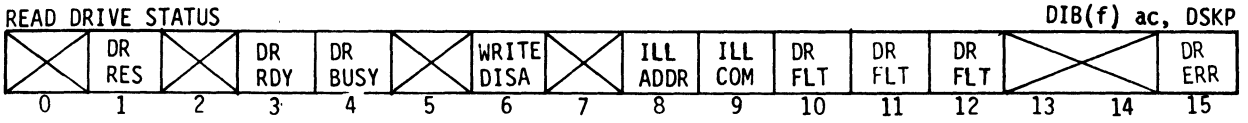


Chart of Accumulator Bit Functions:

Bits	Function
0	Unused.
1	Drive reserved by other processor.
2	Unused.
3	Drive ready.
4	Drive busy. Drive is executing a position command.
5	Unused.
6	Write disabled.
7	Unused.
8	Illegal address. The cylinder address specified exceeds capacity of the drive.
9	Illegal command. A seek command was issued to a busy drive or a write command was issued to a write protected drive.
10-12	Drive Fault.
13-14	Unused.
14	Drive error flag. One or more of bits 8 thru 12 is set to one (1).

3.2.6.1 Drive Error Conditions

Accumulator bits 8-12 and 15, which are transferred to the computer by the DIB instruction, carry disc drive status information to the processor. The accumulator bits and the error conditions flagged by setting of these bits to a one (1) are listed in the chart below.

Accumulator Bit	Error Flag	Error Condition Description
8	ILLEGAL ADDRESS	The cylinder address received by the drive exceeds the capacity of the drive or a seek command was not completed in 500 milliseconds by the drive. An automatic recalibrate is issued by the controller.
9	ILLEGAL COMMAND	A seek command was issued to a busy drive or a write command was issued to a write protected drive.
10-12	DRIVE FAULT	Any drive fault. A drive fault on the selected drive during data transfer terminates operation, sets to 1 (one) the device-done flag and the controller-error flag. If the controller detects a drive fault, it issues a fault-clear command to that drive. If the controller detects a seek error in the drive it issues a recalibrate command to that drive. It also sets to 1 (one) the drive-DONE flag.
15	DRIVE ERROR FLAG	One or more of the error conditions listed above exist.

3.2.7 Read Memory Address Instruction

Instruction Mnemonic: **DIA**[f] ac,**DSKP** (in Alternate Mode 1)

Instruction Function: Loads the contents of the controller's memory address register into bits 0-15 of the specified AC.

Accumulator Format:

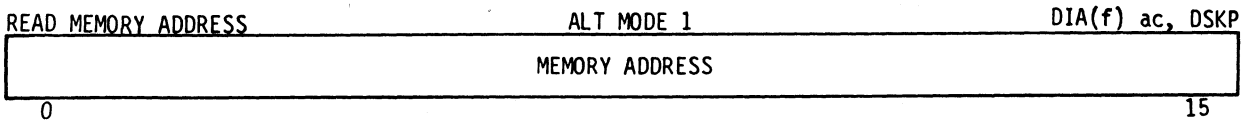


Chart of Accumulator Bit Functions:

Bits	Function
0-15	Memory address of next data channel transfer.

3.2.8 Read Extended Memory Address Instruction

Instruction Mnemonic: **DIB**[f] ac,**DSKP** (in Alternate Mode 1)

Instruction Function: Loads the contents of the controller's extended memory address register (optional) into bits 12-15 of the specified AC.

Accumulator Format:

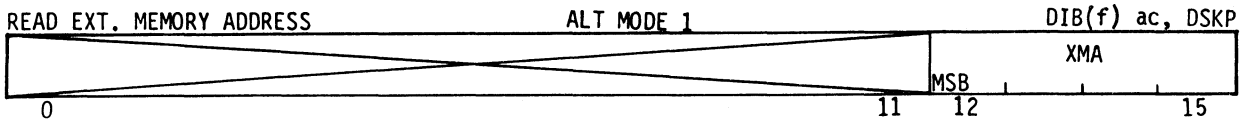


Chart of Accumulator Bit Functions:

Bits	Function
0-11	Unused.
12-15	Extended Memory Address (optional).

3.2.9 Read High-Order ECCR Bits Instruction

Instruction Mnemonic: **DIA[f]** ac,**DSKP** (in Alternate Mode 2)

Instruction Function: Loads the high-order bits of the controller's ECC remainder register into bits 0-15 of the specified AC.

Accumulator Format:

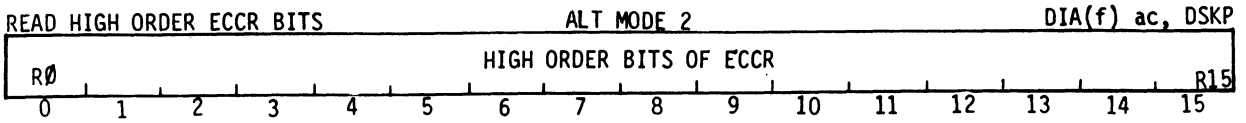


Chart of Accumulator Bit Functions:

Bits	Function
0-15	High-order bits of ECC remainder following a read or verify operation.

3.2.10 Read Low-Order ECCR Bits Instruction

Instruction Mnemonic: **DIB[f]** ac,**DSKP** (in Alternate Mode 2)

Instruction Function: Loads the low-order bits of the controller's ECC remainder register into bits 0-15 of the specified AC.

Accumulator Format:

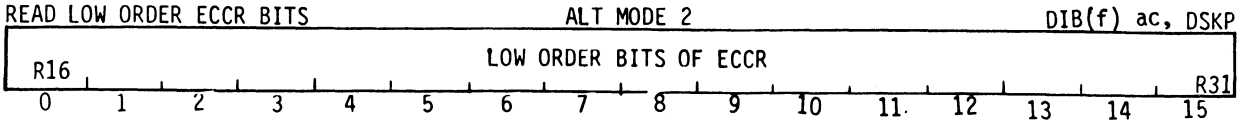


Chart of Accumulator Bit Functions:

Bits	Function
0-15	Low-Order bits of ECC remainder following a read or verify operation.

3.2.11 Read Surface, Sector, Count Instruction

Instruction Mnemonic: **DIC[f] ac,DSKP**

Instruction Function: Loads the contents of the controller's surface address register into bits 1-5 of the specified AC. Loads the contents of the controller's sector-address register into bits 6-10 of the specified AC. Loads the contents of the controller's sector-count register into bits 11-15 of the specified AC.

Accumulator Format:

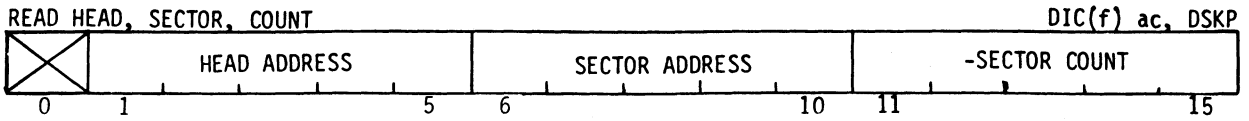


Chart of Accumulator Bit Functions:

Bits	Function
0	Unused.
1-5	Surface address of the sector addressed by bits 6-10.
6-10	Sector address of the sector following the last sector that was transferred.
11-15	Two's complement of the number of sectors remaining to be transferred.

3.3 DISC FORMATTING

Before data transfer operations can take place the surfaces on the disc must be formatted. Formatting records a unique header at the beginning of each sector on the disc. This header contains the information necessary to identify each sector. Figure 3-1 represents the configuration of a formatted sector.

3.3.1 Sector Format

The formatted sector consists of:

- 30 bytes of preamble and sink bit
- 6 bytes of header information
- 2 bytes of header CRC (cyclic redundancy code)
- 2 bytes of gap
- 30 bytes of data splice preamble and sink bit
- 512 bytes of data storage
- 4 bytes of ECC (error correction code)
- 2 bytes of postamble

The 6 bytes of header information contain address information used by the controller to locate the desired sector for a data transfer operation. The cylinder address occupies 10 bits of the first word of the header. The first word of the header also contains a bad sector flag and an alternate sector flag of one bit each. Surface address (5-bit), sector address (5-bit) and alternate sector address (5-bit) occupy the second word of the header. Word three of the header contains a 5-bit alternate surface address and a 10-bit alternate cylinder address. The header is completed by a word of CRC that ensures error-free reading of the header.

If a sector cannot support error-free data, the Format/Surface Analysis Program sets the bad-sector flag or the alternate-sector flag. If the bad-sector flag is set to one (1) operation will be terminated. If the alternate-sector flag is set to one (1), an alternate-sector address is provided.

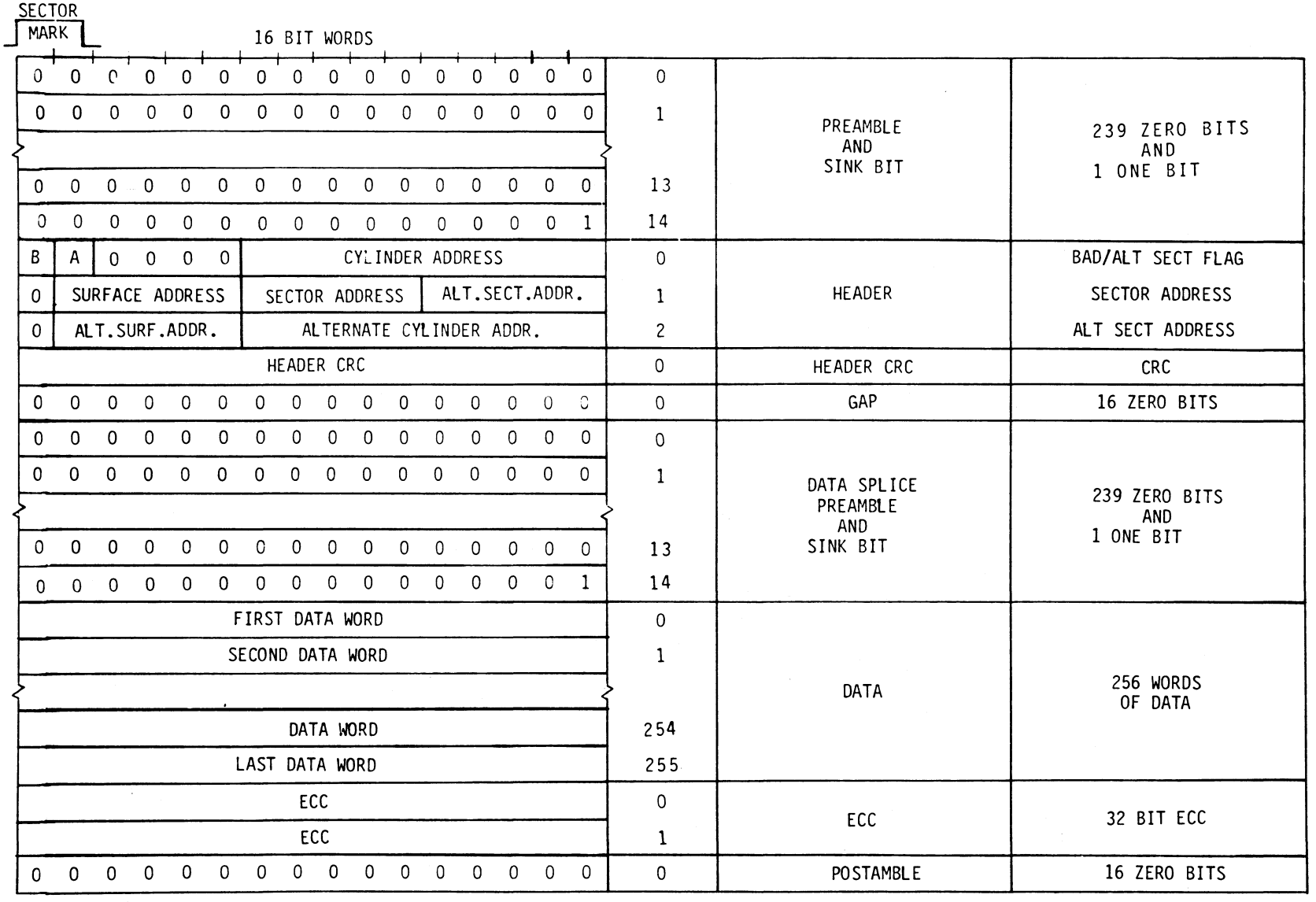


Figure 3-1. Configuration of a Formatted Sector

3.3.2 Format Programming

The format command causes complete reformatting of the sector(s) specified. Header information is provided from the controller's address register. When a sector is formatted all data in that sector is lost (the sector data bytes are filled with 0's).

The write-header command is provided to set flags, write alternate sector address, or provide for interleaving of sectors. The write-header command uses three words from computer memory as a source of header information. This command does not destroy the data in that sector.

For data-transfer commands the controller reads the sector headers passing under the selected disc drive head. It checks flags, address and CRC.

- A CRC error causes a retry on the next header
- A cylinder/surface address error terminates the operation by setting the respective error flags

If the cylinder, surface and sector address match:

- A bad-sector flag terminates the operation
- An alternate-sector flag causes the controller to find the sector designated by the alternate-sector address

If neither flag is set, data transfer commences. See Figure 3-2 for a flowchart of this operation.

For format, write-header, and read-format operations the controller synchronizes to the index mark, and then counts the sector marks to find the desired sector.

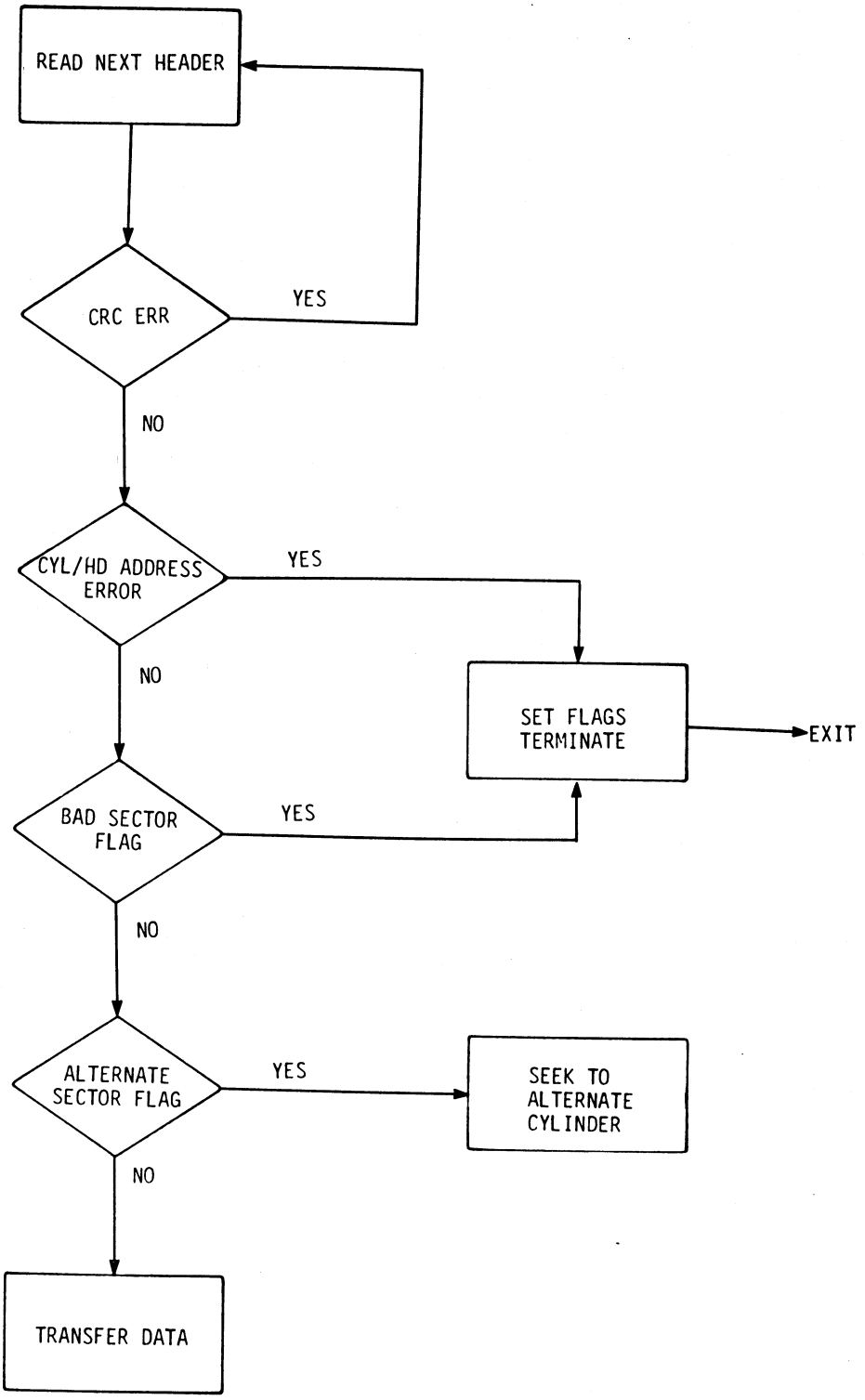


Figure 3-2. Format Programming Flowchart

3.4 DATA TRANSFER PROGRAMMING

Execution of a data transfer between the disc and memory requires use of a series of commands to ensure that all information necessary for the transfer has been conveyed to all devices involved. Activities involved in a data transfer include:

- drive selection
- status checks on that drive and the controller
- drive head positioning
- issuing of a read or write command
- specification of disc surface and sector address
- specification of the memory address for data transfer
- start operation

3.4.1 Drive Command Operation Procedure

Drive Commands are: recalibrate, seek, trespass and release. All may be programmed using the following procedure:

1. Check the controller status by issuing a DIA (Read Controller Status) instruction. In order to proceed, the controller status transferred to the processor accumulator must contain the control-full flag (bit 0) set to zero (0), indicating that the previous drive command has been transmitted to that drive. If the control-full flag is set to one (1) all DOA instructions will be ignored.

2. Select the drive and specify the drive command by issuing a DOA (Specify Command and Drive) instruction. The processor accumulator should contain the drive number in bits 9 and 10. This information will be transferred to the controller's drive select register. Bits 5 through 8 of the accumulator should contain the drive command to be transferred to the controller's command register.

3. Read the disc drive status by issuing a DIB (Read Drive Status) instruction. The drive status information transferred from the controller indicates whether the drive is ready; whether the drive is reserved by the other processor in the system (if any); whether any drive faults exist; and whether the drive is busy with a previous drive command. The drive will reject all commands if it is not ready, is busy, or has been reserved by the other processor.

4. The desired cylinder number is specified by issuing a DOCP (Specify Cylinder) instruction. The P (Pulse) control function sets the control-full flag to one (1) and initiates the command transfer to the drive. Once the command is transferred to the drive, the control-full flag is cleared. Completion of the command sets the drive-done flag to one (1), causing an interrupt to the controller (if the controller-busy flag is not set to 1). If the drive is not ready, is busy or has been reserved for the other processor when the DOCP instruction is issued, the command will be rejected by setting the drive-done flag to one (1) and clearing the control-full flag to zero (0).

NOTE

Trespass and recalibrate commands are issued similarly.

3.4.2 Data Transfer Procedure

Read/write commands can be issued without waiting for the completion of the seek operation. Once the seek operation has been initiated, proceed to program data transfer as follows:

1. Check the device (controller) busy flag by issuing a Skip-if-BUSY-Flag-is-Nonzero-I/O instruction. Verify that no data transfer is in progress (BUSY = 0). No new data transfer may be initiated if the previous data transfer is still in progress.

2. Check controller status by issuing a DIA (Read Controller Status) instruction. In order to proceed, the controller status transferred to the processor accumulator must contain the control-full flag (bit 0) set to zero (0), indicating that the previous drive command has been transmitted to that drive. If the control-full flag is set to one (1), all DOA instructions will be ignored.

3. Select the drive and specify a read/write (or verify) command by issuing a DOA (Specify Command and Drive) instruction. The processor accumulator should contain the drive number in bits 9 and 10. This information will be transferred to the controller's drive-select register. Bits 5 through 8 of the accumulator should contain a read/write or verify command (0000/1110 or 1100) to be transferred to the controller's command register.

4. Read the disc drive status by issuing a DIB (Read Drive Status) instruction. Check the status to verify that the disc drive is ready, that it is not reserved by the other processor (if any), and that there is no drive fault. For a write operation, that drive must not be write-protected.

5. The desired starting surface, sector address and sector count is specified by issuing a DOC (Specify Surface, Sector and Sector Count) instruction. Bits 1-5 of the processor accumulator should contain the surface address to be transferred to the controller's surface-address register. Bits 6-10 of the accumulator should contain the sector address to be transferred to the controller's sector-address register. Bits 11-15 of the accumulator should contain the sector count to be transferred into the controller's sector count register.

6. Issue a DOBS to specify the memory address to be used in the first DMA transfer. The S (Start) control function sets the device-busy flag to one (1), clears to zero (0) the device-done flag, starts a one-second timer and initiates the data transfer operation.

   The controller finds the desired sector on the specified surface and performs the data transfer between memory and the disc drive. Data transfer continues until sector count overflows, at which time transfer operation terminates. Termination of data transfer causes BUSY to clear to zero (0), sets the device-done to one (1), and generates an interrupt to the processor.

3.4.3 Dual Processor Data Transfer Procedure

In a dual processor system it may be desirable to release the disc drive after a data transfer operation. This allows access to the disc drive by the other processor in the system.

To release the disc drive from reserved status, proceed as follows:

1. Check the controller status by issuing a DIA (Read Controller Status) instruction. The controller status transferred to the processor accumulator must contain the control-full flag (bit 0) set to zero (0) in order to proceed.

2. Select the desired drive and specify a release command by issuing a DOAP (Specify Command and Drive) instruction. The P (Pulse) control function sets the control-full flag to one (1) and initiates the release command to that drive. Once the release command is transferred to that drive the control-full flag is cleared to zero (0).

3.4.4 Programming Flowcharts

Figures 3-3 through 3-5 are flowcharts of programming procedures for drive command operations, data transfer operations and interrupt operations. Each procedure is flowcharted in the following figures:

Figure 3-3. Drive Command Operation Programming Flowchart

Figure 3-4. Data Transfer Operation Programming Flowchart

Figure 3-5. Interrupt Processing Programming Flowchart

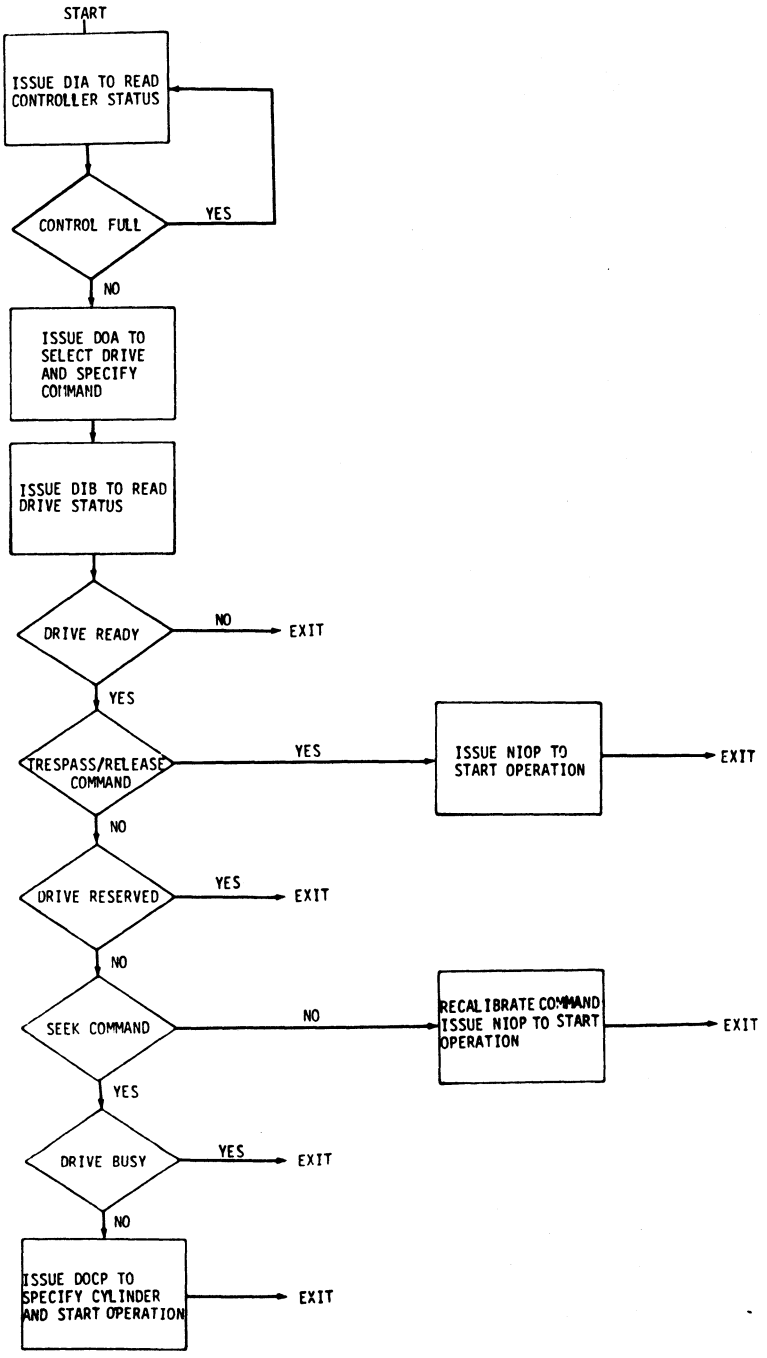


Figure 3-3. Drive Command Operation Programming Flowchart

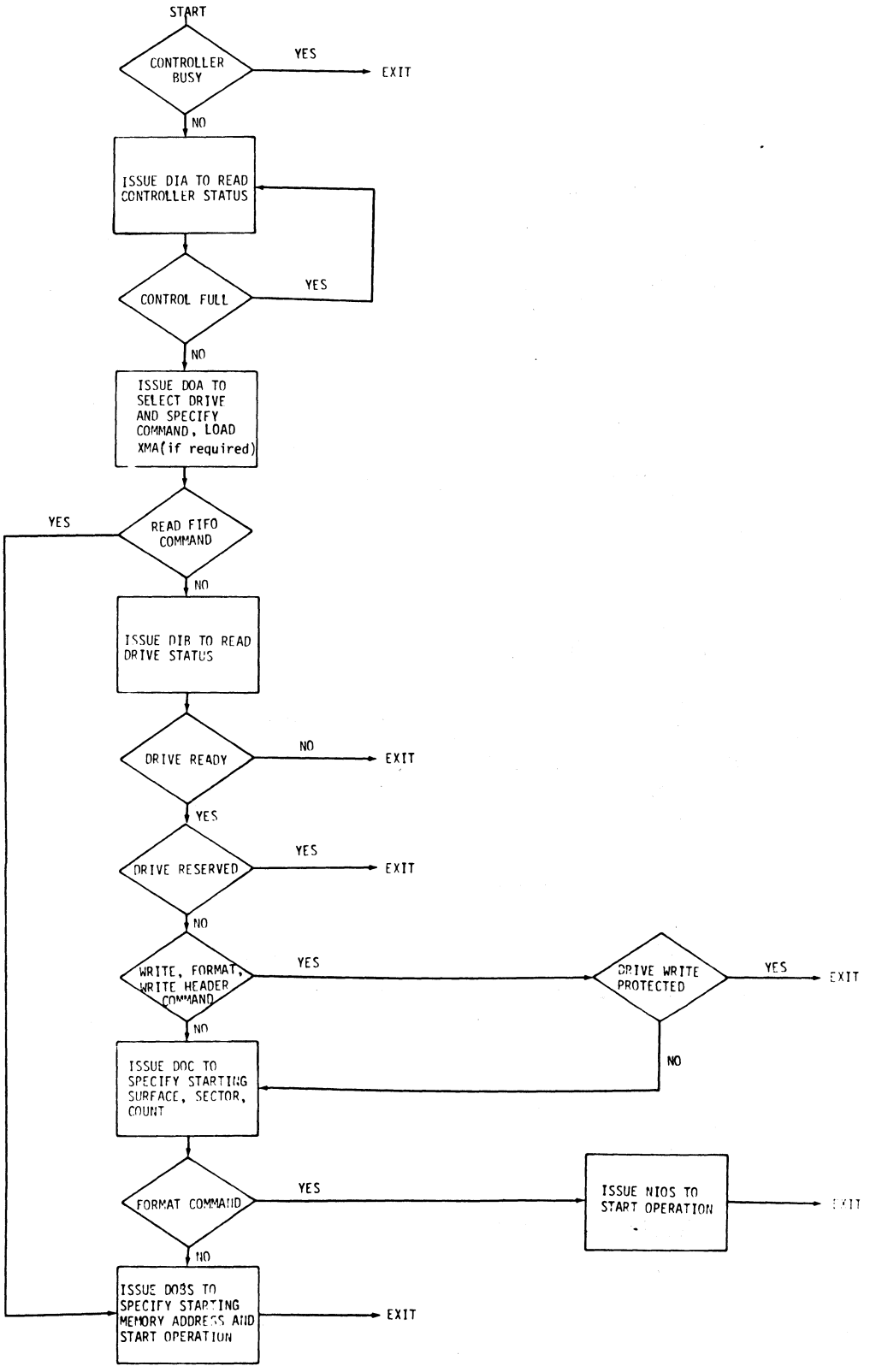


Figure 3-4. Data Transfer Operation Programming Flowchart

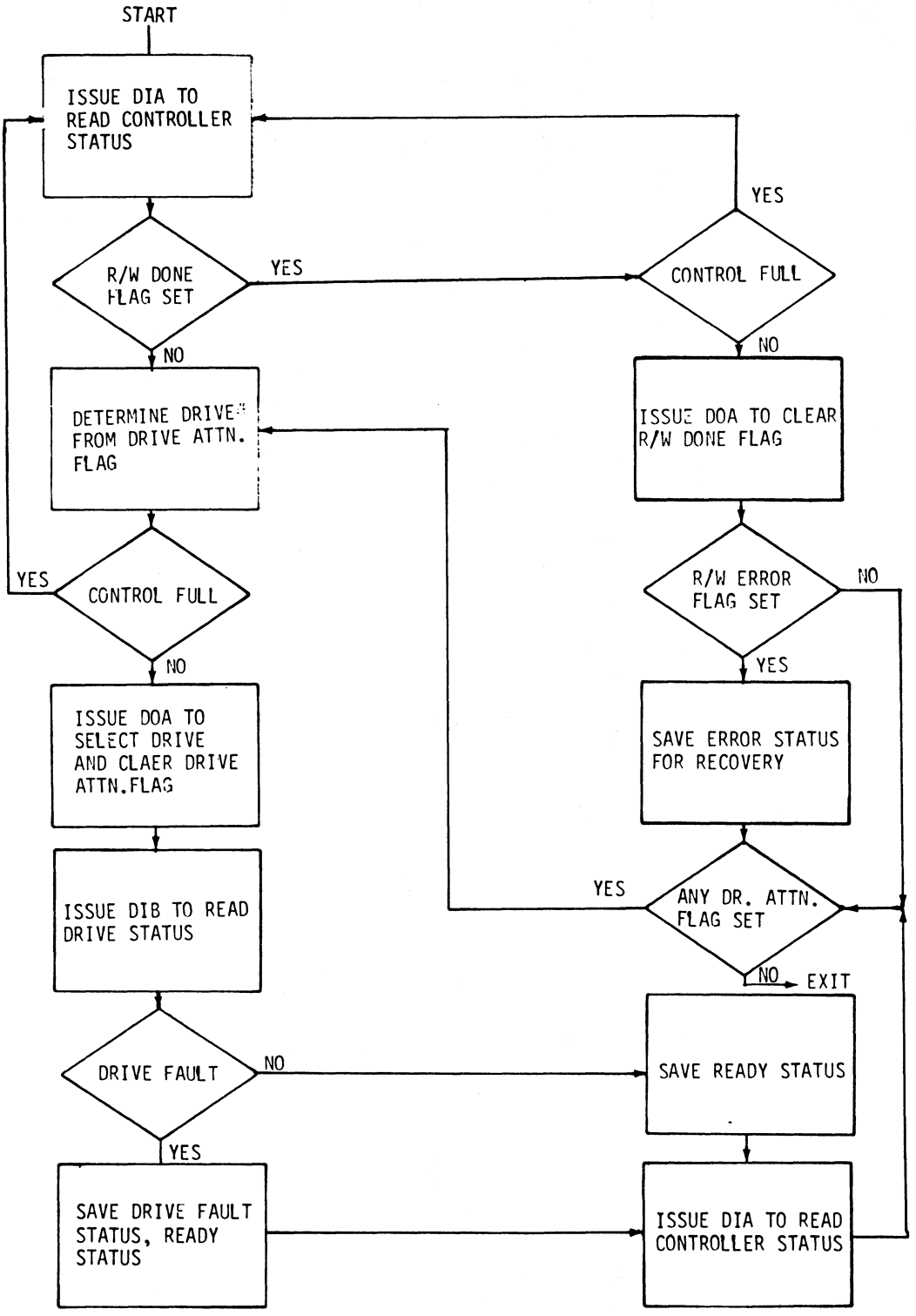


Figure 3-5. Interrupt Processing Programming Flowchart

3.5 DATA ERROR DETECTION AND CORRECTION

When the controller writes data into a sector, it generates a 4-byte Error Correction Code (ECC) checkword immediately after the last data word (see Figure 3-1, Configuration of a Formatted Sector). When the controller reads data from a sector it generates an ECC remainder from the 512 bytes of data and the four bytes of ECC checkword. If the remainder generated is nonzero, an error has occurred in data transfer. The ECC error flag is set to one (1) in the controller.

The ECC feature detects all errors contained within 21 contiguous bits. It also provides for software correction of errors within 11 contiguous bits. A number of additional errors may also be detected; however, correction is not guaranteed since there is a small possibility that the correction algorithm will produce erroneous correction on data strings containing errors that exceed 11 bits. There is also a very small class of errors that cannot be detected by this ECC-generation routine.

3.5.1 Error Detection Procedure

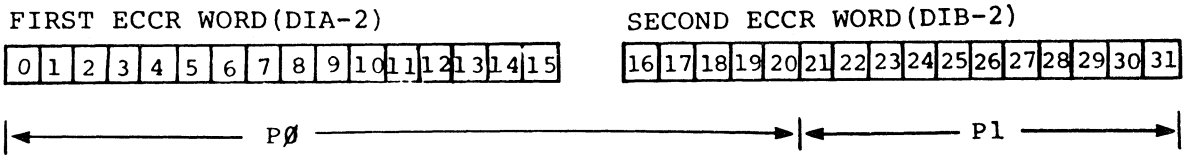
To detect errors using the ECC remainder (ECCR) generated when the data transfer took place, proceed as follows:

A) Use a DIA instruction in Alternate Mode 2 (Read-High-Order-ECCR bits) to read the high-order word of the controller's ECCR Register into bits 0-15 of the specified processor accumulator.

B) Use a DIB instruction in Alternate Mode 2 (Read-Low-Order-ECCR bits) to read the low-order word of the controller's ECCR Register into bits 0-15 of the specified processor acccumulator.

C) To check for a detected data transfer error and for correctability proceed as follows:

1) The 32 bits of the two ECCR words are grouped using the identifiers P0 and P1. P0 consists of the first 21 bits of the two ECCR words and P1 consists of the last 11 bits of the two ECCR words as illustrated below:



2) Test for the following conditions in P0 and P1.

   a) If both P0 and P1 are EQUAL to zero (0) then no error has been detected. Exit the routine.

   b) If P0 is NOT EQUAL to zero (0) and P1 is EQUAL to zero (0) or if P0 is EQUAL to zero (0) and P1 is NOT EQUAL to zero (0) the error is not correctable. Exit the routine.

   c) If both P0 and P1 are NOT EQUAL to zero (0) proceed to step 3 below.

3) Rotate P0 left N times until P0 (bits 0-9) is equal to zero (0). See Figure 3-6 for an illustration of this procedure.

4) If N is greater than or equal to zero and less than or equal to 21 ($0 \leq N \leq 21$) save the value of N and the error pattern. Then proceed to step 5 below. If N is greater than 21 the error is not correctable; exit the routine.

5) Rotate P1 and "exclusive OR" bit 30 with bit 21 M times until P1 (bits 21-31) are equal to the error pattern. See Figure 3-7 for an illustration of this procedure.

6) If M is greater than or equal to zero and less than or equal to 2047 ($0 \leq M \leq 2047$) proceed to the error correction procedure below. If M is greater than 2047 the error is not correctable; exit the routine.

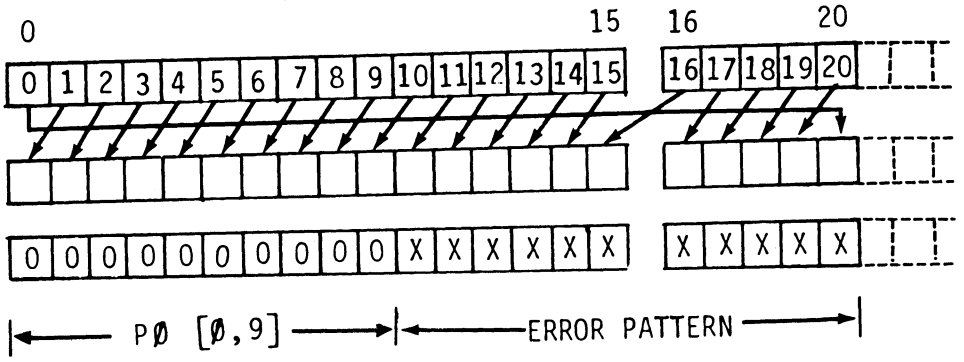


Figure 3-6. Rotation of P0 Left N Times

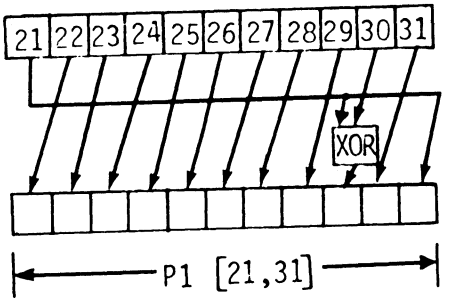


Figure 3-7. Rotation and Exclusive OR of P1

3.5.2 Error Correction Procedure

To compute bit displacement of the eleven-bit error burst, determine location of the error, and make calculated corrections proceed as follows:

1) If the value of M, calculated in steps 5 and 6 above, is greater than or equal to the value of N, calculated in steps 3 and 4 above, proceed to step 3 below. If the value of M is less than the value of N proceed to step 2 below.

2) To calculate the bit offset (R) perform the following calculations:

$$R = 19 \cdot (N-M) \cdot \text{Modulo } 21$$
$$X = 2047 \cdot R + M$$

Proceed to step 4 below.

3) To calculate the bit offset (R) perform the following calculations:

$$R = 195 \cdot (M-N) \cdot \text{Modulo } 2047$$
$$X = 21 \cdot R + N$$

Proceed to step 4 below.

4) To calculate the bit displacement of the burst error from the start of the sector (D) make the following calculations:

$$D = X - 36812$$

Proceed to step 5.

5) Test the bit displacement calculated in step 4 for a greater than zero condition ($D > 0$). If the displacement is greater than zero proceed to step 6 below. If the displacement is equal to or less than zero, proceed to step 7 below.

6) Test the bit displacement for equal to or greater than 4128 ($D \geq 4128$). If the displacement is equal to or is greater than 4128, proceed to step 8 below. If the displacement is less than 4128, proceed to step 9 below.

7) Test the bit displacement for equal to or less than -11 ($D \geq -11$). If the displacement is equal to or less than -11, proceed to step 8 below. If the displacement is greater than -11, proceed to step 13 below.

8) This error is not correctable. The bit displacement indicates the error has occurred outside the sector. Exit the routine.

9) Test the bit displacement for equal to or greater than 4096 ($D \geq 4096$). If the displacement is equal to or greater than 4096, proceed to step 11 below. If the displacement is less than 4096, proceed to step 10 below.

10) The error is in the Error Correction Code. The data transferred is correct. Exit the routine.

11) Test the bit displacement for greater than 4085 ($D > 4085$). If the displacement is greater than 4085, proceed to step 12 below. If the displacement is equal to or less than 4085, proceed to step 17 below.

12) Perform the following calculation:

$$S = D - 4085$$

Set to zero "S" number of the least significant bits of the error pattern. Proceed to step 17 below.

13) Test the most significant bit of the error pattern for equal to one (MSB = 1). If the MSB equals one (1), return to step 8 above. If the MSB equals zero (0), go to step 14 below.

14) Shift the error pattern left one position. Proceed to step 15 below.

15) Perform the following calculation:

$$D = D + 1$$

Proceed to step 16 below.

16) Test the bit displacement for equal to zero ($D = 0$). If the displacement is equal to zero, proceed to step 17 below. If the displacement is not equal to zero, return to step 13 above.

17) Perform the calculation below to properly align the bit displacement:

$$D = 16Q + R$$

(where Q = Word Offset, and R = Bit Offset)

Figure 3-8 illustrates the word and bit offsets as well as replacement of the corrected data.

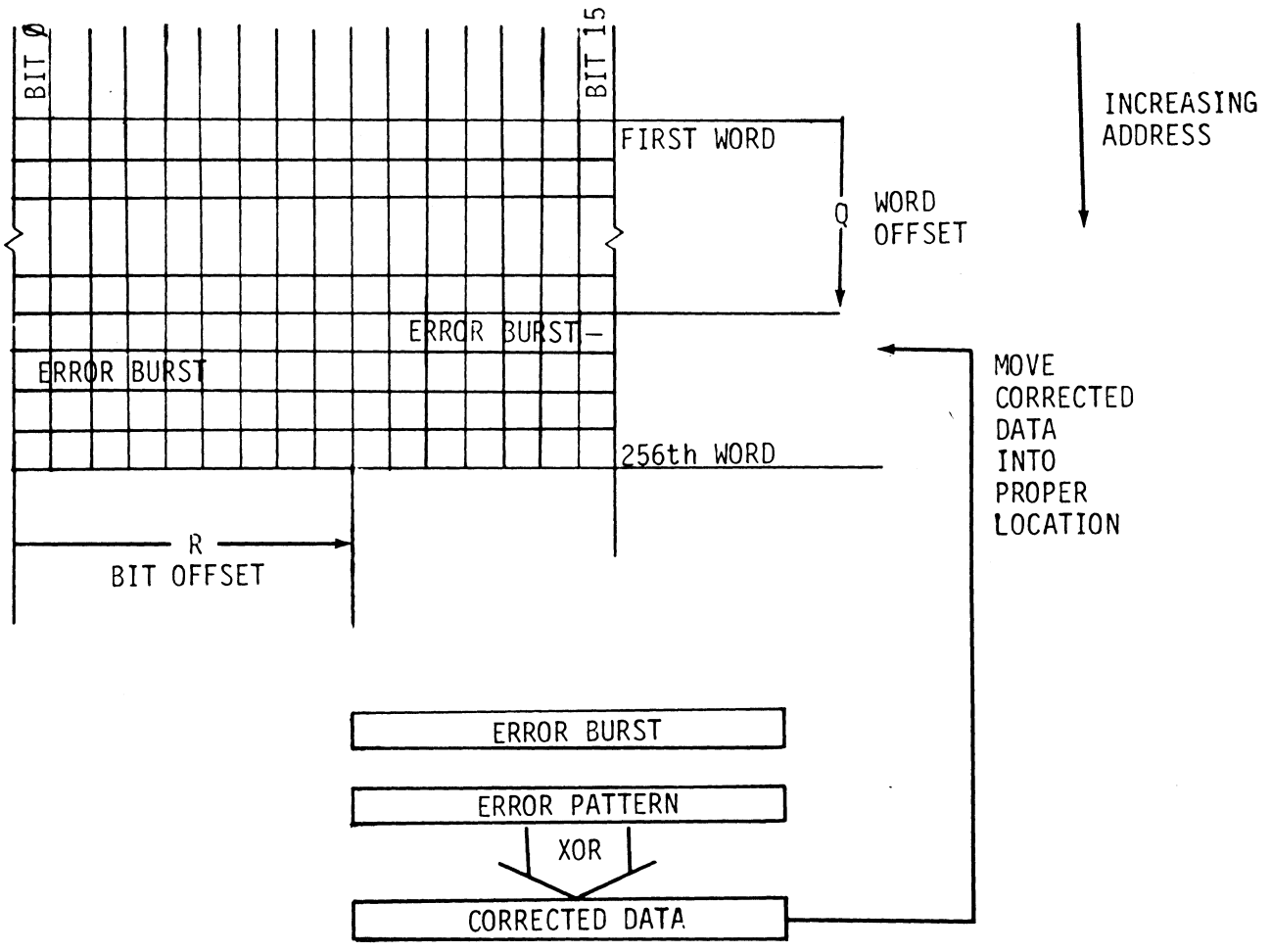


Figure 3-8. Word and Bit Offsets and Data Replacement Procedure

3.5.3 Error Detection and Correction Flowchart

Figure 3-9 is a flowchart illustrating the procedures for error detection and correction.

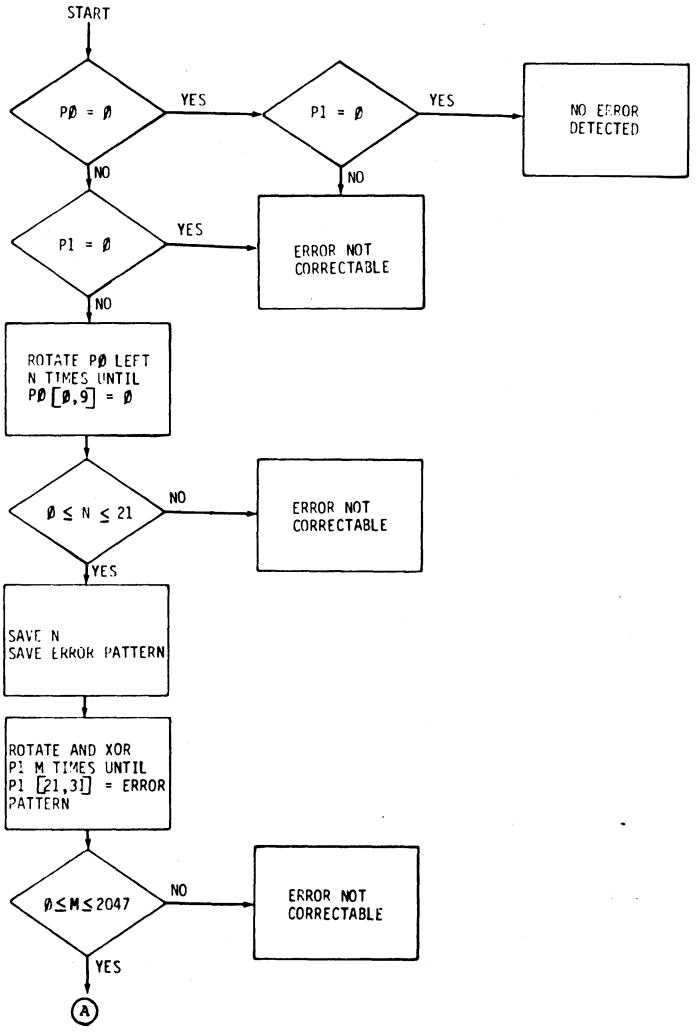


Figure 3-9. Error Detection and Correction Flowchart (Sheet 1)

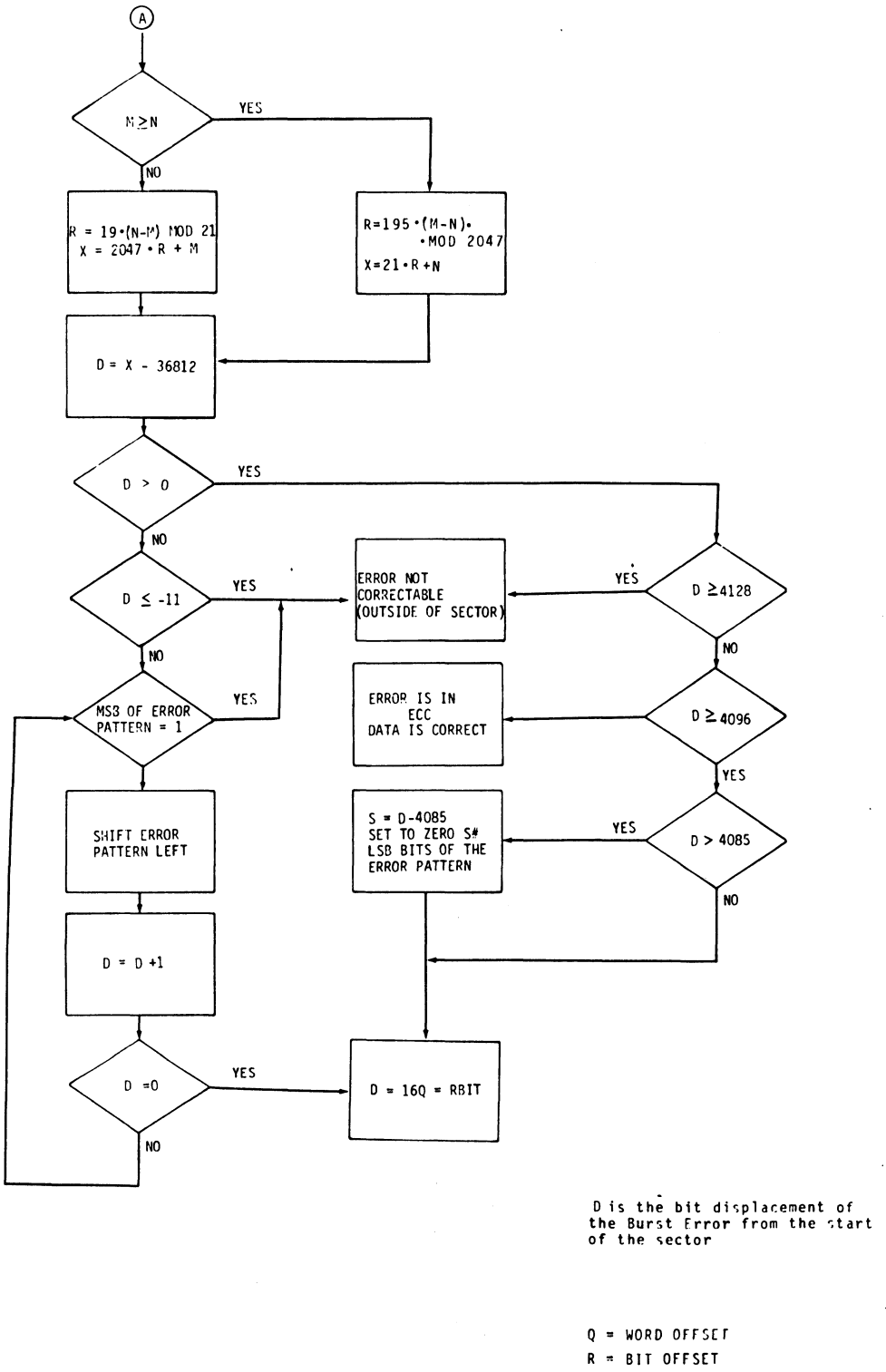
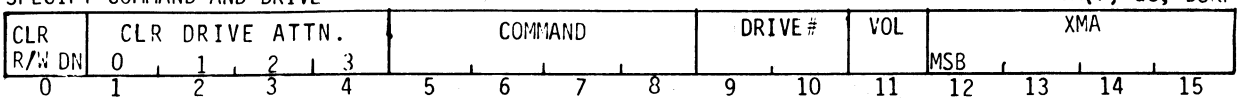


Figure 3-9. Error Detection and Correction Flowchart (Sheet 2)

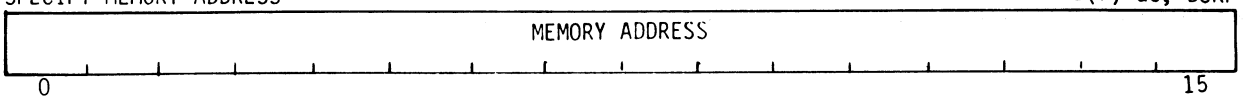
Appendix A
ACCUMULATOR FORMATS

This appendix contains a summary of all the accumulator formats showing the appropriate I/O instruction and the assembly language instruction format.

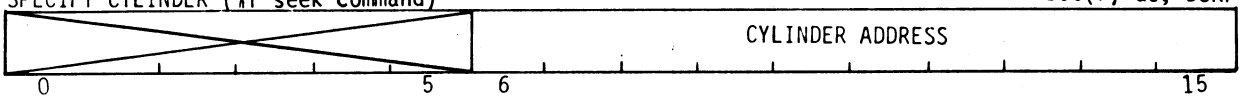
SPECIFY COMMAND AND DRIVE — DOA(f) ac, DSKP



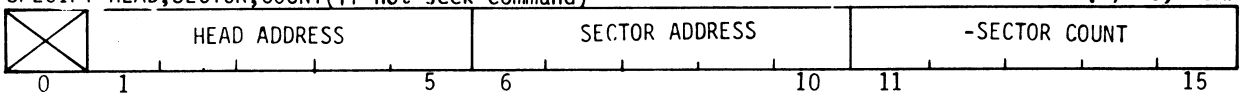
SPECIFY MEMORY ADDRESS — DOB(f) ac, DSKP



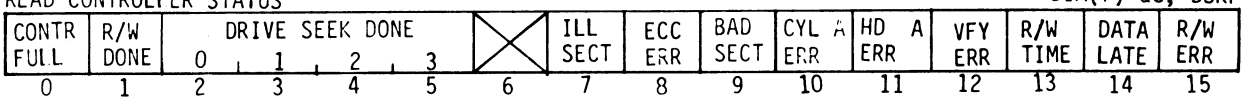
SPECIFY CYLINDER (if seek command) — DOC(f) ac, DSKP



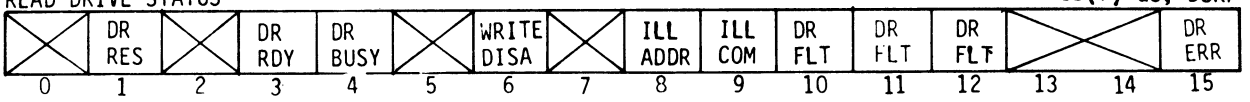
SPECIFY HEAD,SECTOR,COUNT(if not seek command) — DOC(f) ac, DSKP



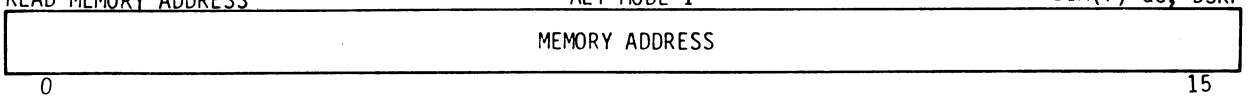
READ CONTROLLER STATUS — DIA(f) ac, DSKP



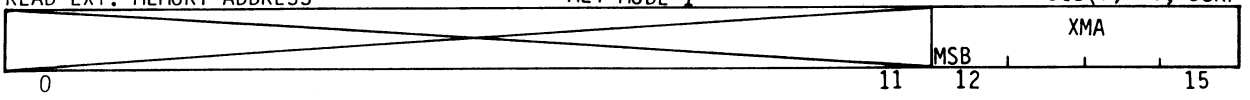
READ DRIVE STATUS — DIB(f) ac, DSKP



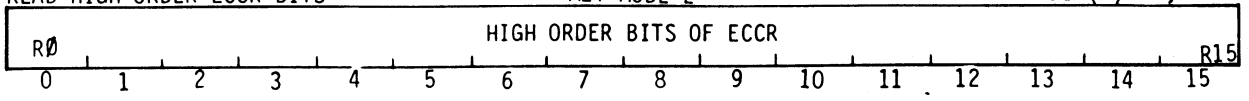
READ MEMORY ADDRESS — ALT MODE 1 — DIA(f) ac, DSKP



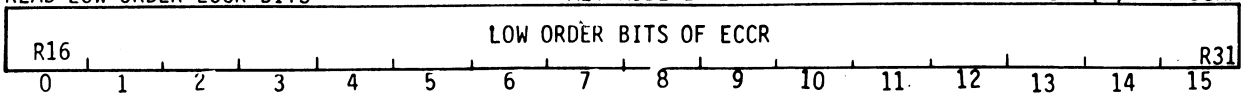
READ EXT. MEMORY ADDRESS — ALT MODE 1 — DIB(f) ac, DSKP



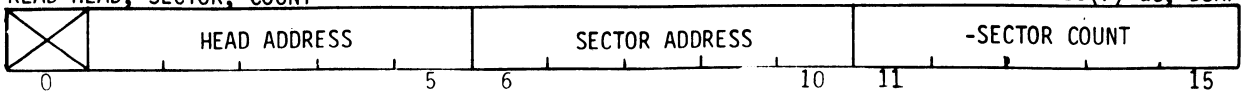
READ HIGH ORDER ECCR BITS — ALT MODE 2 — DIA(f) ac, DSKP



READ LOW ORDER ECCR BITS — ALT MODE 2 — DIB(f) ac, DSKP



READ HEAD, SECTOR, COUNT — DIC(f) ac, DSKP



Appendix B

CONFIGURATION CHART EXAMPLES

This appendix contains Head PROM configuration chart samples for CMD32, CMD64, CMD96, MMD80, SMD80, and SMD300 disc drives, and sector configuration charts for 32 and 24 sectors.

DRIVE Ø								CMD 32				DRIVE 1								CMD 64				DRIVE 2								CMD 96				DRIVE 3											
VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX
H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12		1	2	3	4	7	6	5	9	10	11	12
0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0		0		0
0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	1				0
0	0	0	0	0	0	1	0	1	1	0	0	0	0	1	0	0	0	1	0	1	1	0	0	0	1	0	0	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1	0				0
0	0	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	1	1				0
0	0	0	0	0	1	0	0	1	1	0	0	0	0	1	0	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	1	0	0				0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	1	0	0	1	0	1	1	1	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0	1	1	0	0	1	0	1				0
0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	0	1	1	0	0	0	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0	0	1	1	0				0
0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0	1	1	0	0	1	1	1				0
0	0	0	0	1	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	1	1	0	0	0	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0	1	0	0	0				0
0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	0	1	1	1	0	0	0	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	0	1				0
0	0	0	0	1	0	1	0	1	1	0	0	0	0	1	0	1	0	1	0	1	1	0	0	0	1	0	0	1	0	1	0	1	1	0	0	0	1	1	0	1	0	1	0				0
0	0	0	0	1	0	1	1	1	1	0	0	0	0	1	0	1	0	1	1	1	1	0	0	0	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	1	0	1	1				0
0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	0	1	1	0	0	1	1	0	0	0	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	1	1	0	0				0
0	0	0	0	1	1	0	1	1	1	0	0	0	0	1	0	1	1	0	1	1	1	0	0	0	1	0	0	1	1	0	1	1	1	0	0	0	1	1	0	1	1	0	1				0
0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0	1	1	1	0	1	1	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	1	1	0	1	1	1	0				0
0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	1	0	0	1	1	1	1	1	1	0	0	0	1	1	0	1	1	1	1				0
0	0	0	1	0	0	0	0	1	1	0	1	0	0	1	1	0	0	0	0	1	1	0	1	0	1	0	1	0	0	0	0	1	1	0	1	0	1	1	1	0	0	0	0				1
0	0	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	1	1	0	1	0	1	0	1	0	0	0	1	1	1	0	1	0	1	1	1	0	0	0	1				1
0	0	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0	1	0	1	0	1	0	0	1	0	1	1	0	1	0	1	1	1	0	0	1	0				1
0	0	0	1	0	0	1	1	1	1	0	1	0	0	1	1	0	0	1	1	1	1	0	1	0	1	0	1	0	0	1	1	1	1	0	1	0	1	1	1	0	0	1	1				1
0	0	0	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0	1	1	0	1	0	1	1	1	0	1	0	0				1
0	0	0	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1	1	1	0	1	0	1	1	1	0	1	0	1				1
0	0	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1	1	0				1
0	0	0	1	0	1	1	1	1	1	0	1	0	0	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1	1	1	0	1	0	1	1	1	0	1	1	1				1
0	0	0	1	1	0	0	0	1	1	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	1	0	1	1	0	0	0	1	1	0	1	0	1	1	1	1	0	0	0				1
0	0	0	1	1	0	0	1	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	0	1	1	1	0	1	0	1	1	1	1	0	0	1				1
0	0	0	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	1	0	1	0	1	1	1	1	0	1	0				1
0	0	0	1	1	0	1	1	1	1	0	1	0	0	1	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1	1	1	1	0	1	0	1	1	1	1	0	1	1				1
0	0	0	1	1	1	0	0	1	1	0	1	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	1	1	1	0	0	1	1	0	1	0	1	1	1	1	1	0	0				1
0	0	0	1	1	1	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1	1	1	0	1	0	1	1	1	1	1	0	1				1
0	0	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	1	0	1	0	1	1	1	1	0	1	1	0	1	0	1	1	1	1	1	1	0				1
0	0	0	1	1	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1	1	1	0	1	0	1	1	1	1	1	1	1				1

SHEET 1

SHEET 2

DRIVE Ø (CMD 32)	VOL	H	15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USB	G	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	USA	F	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	HØ	E	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	H1	D	4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	H2	C	7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	H3	B	6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	1
	H4	A	5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	1
	LAST H	4	9	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	ILL H	3	10	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	INHRST H	2	11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	HX	1	12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DRIVE 1 (CDM 64)	VOL	H	15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USB	G	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	USA	F	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	HØ	E	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	H1	D	4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	H2	C	7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	H3	B	6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	H4	A	5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	LAST H	4	9	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	ILL H	3	10	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	INHRST H	2	11	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	HX	1	12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DRIVE 2 (CDM 96)	VOL	H	15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USB	G	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USA	F	2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	HØ	E	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	H1	D	4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	H2	C	7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	H3	B	6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	H4	A	5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	LAST H	4	9	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	ILL H	3	10	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	INHRST H	2	11	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	HX	1	12	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
DRIVE 3	VOL	H	15	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USB	G	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	USA	F	2	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	HØ	E	3	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	H1	D	4	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	H2	C	7	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
	H3	B	6	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	H4	A	5	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	LAST H	4	9																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	ILL H	3	10																	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	INHRST H	2	11																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	HX	1	12	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

DRIVE Ø							MMD / SMD	30 / 80				DRIVE 1							SMD	300				DRIVE 2												DRIVE 3											
VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX
H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0		0		0	0	1	1	0	0	0	0	0		0		0
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	1				0	0	1	1	0	0	0	0	1				0
0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	1	0				0	0	1	1	0	0	0	1	0				0
0	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	1	1				0	0	1	1	0	0	0	1	1				0
0	0	0	0	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1	0	0	0	1	0	0				0	0	1	1	0	0	1	0	0				0
0	0	0	0	0	1	0	1	1	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	1	0	1				0	0	1	1	0	0	1	0	1				0
0	0	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	0	0	0	0	0	0	1	0	0	0	1	1	0				0	0	1	1	0	0	1	1	0				0
0	0	0	0	0	1	1	1	1	1	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	1	0	0	0	1	1	1				0	0	1	1	0	0	1	1	1				0
0	0	0	0	1	0	0	0	1	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0				0	0	1	1	0	1	0	0	0				0
0	0	0	0	1	0	0	1	1	1	0	0	0	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0	0	1				0	0	1	1	0	1	0	0	1				0
0	0	0	0	1	0	1	0	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	1	0	0	1	0	1	0				0	0	1	1	0	1	0	1	0				0
0	0	0	0	1	0	1	1	1	1	0	0	0	0	1	0	1	0	1	1	0	0	0	0	0	1	0	0	1	0	1	1				0	0	1	1	0	1	0	1	1				0
0	0	0	0	1	1	0	0	1	1	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	1	0	0	1	1	0	0				0	0	1	1	0	1	1	0	0				0
0	0	0	0	1	1	0	1	1	1	0	0	0	0	1	0	1	1	0	1	0	0	0	0	0	1	0	0	1	1	0	1				0	0	1	1	0	1	1	0	1				0
0	0	0	0	1	1	1	0	1	1	0	0	0	0	1	0	1	1	1	0	0	0	0	0	0	1	0	0	1	1	1	0				0	0	1	1	0	1	1	1	0				0
0	0	0	0	1	1	1	1	1	1	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	1	0	0	1	1	1	1				0	0	1	1	0	1	1	1	1				0
0	0	0	1	0	0	0	0	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0				1	0	1	1	1	0	0	0	0				1
0	0	0	1	0	0	0	1	1	1	0	1	0	0	1	1	0	0	0	1	0	0	0	1	0	1	0	1	0	0	0	1				1	0	1	1	1	0	0	0	1				1
0	0	0	1	0	0	1	0	1	1	0	1	0	0	1	1	0	0	1	0	1	0	0	1	0	1	0	1	0	0	1	0				1	0	1	1	1	0	0	1	0				1
0	0	0	1	0	0	1	1	1	1	0	1	0	0	1	1	0	0	1	1	1	1	0	1	0	1	0	1	0	0	1	1				1	0	1	1	1	0	0	1	1				1
0	0	0	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0				1	0	1	1	1	0	1	0	0				1
0	0	0	1	0	1	0	1	1	1	0	1	0	0	1	1	0	1	0	1	1	1	0	1	0	1	0	1	0	1	0	1				1	0	1	1	1	0	1	0	1				1
0	0	0	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1	0	1	0	1	0	1	1	0				1	0	1	1	1	0	1	1	0				1
0	0	0	1	0	1	1	1	1	1	0	1	0	0	1	1	0	1	1	1	1	1	0	1	0	1	0	1	0	1	1	1				1	0	1	1	1	0	1	1	1				1
0	0	0	1	1	0	0	0	1	1	0	1	0	0	1	1	1	0	0	0	1	1	0	1	0	1	0	1	1	0	0	0				1	0	1	1	1	1	0	0	0				1
0	0	0	1	1	0	0	1	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0	1	0	1	0	1	1	0	0	1				1	0	1	1	1	1	0	0	1				1
0	0	0	1	1	0	1	0	1	1	0	1	0	0	1	1	1	0	1	0	1	1	0	1	0	1	0	1	1	0	1	0				1	0	1	1	1	1	0	1	0				1
0	0	0	1	1	0	1	1	1	1	0	1	0	0	1	1	1	0	1	1	1	1	0	1	0	1	0	1	1	0	1	1				1	0	1	1	1	1	0	1	1				1
0	0	0	1	1	1	0	0	1	1	0	1	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	1	1	1	0	0				1	0	1	1	1	1	1	0	0				1
0	0	0	1	1	1	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1				1	0	1	1	1	1	1	0	1				1
0	0	0	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	0	1	0	1	0	1	1	1	1	0				1	0	1	1	1	1	1	1	0				1
0	0	0	1	1	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	0	1	0	1	0	1	1	1	1	1				1	0	1	1	1	1	1	1	1				1

SHEET 1

DRIVE Ø (SMD 80)												DRIVE 1 (SMD 300)												DRIVE 2												DRIVE 3											
VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX	VOL	USB	USA	HØ	H1	H2	H3	H4	LAST H	ILL H	INHRST H	HX
H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1	H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12	15	1	2	3	4	7	6	5	9	10	11	12
1	0	0	0	0	0	0	0	1	1	0	1	1	0	1	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0	0	0				1	1	1	1	0	0	0	0	0				1
1	0	0	0	0	0	0	1	1	1	0	1	1	0	1	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	0	1				1	1	1	1	0	0	0	0	1				1
1	0	0	0	0	0	1	0	1	1	0	1	1	0	1	0	0	0	1	0	1	1	0	1	1	1	0	0	0	0	1	0				1	1	1	1	0	0	0	1	0				1
1	0	0	0	0	0	1	1	1	1	0	1	1	0	1	0	0	0	1	1	1	1	0	1	1	1	0	0	0	0	1	1				1	1	1	1	0	0	0	1	1				1
1	0	0	0	0	1	0	0	1	1	0	1	1	0	1	0	0	1	0	0	1	1	0	1	1	1	0	0	0	1	0	0				1	1	1	1	0	0	1	0	0				1
1	0	0	0	0	1	0	1	1	1	0	1	1	0	1	0	0	1	0	1	1	1	0	1	1	1	0	0	0	1	0	1				1	1	1	1	0	0	1	0	1				1
1	0	0	0	0	1	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1	1	0	1	1	1	0	0	0	1	1	0				1	1	1	1	0	0	1	1	0				1
1	0	0	0	0	1	1	1	1	1	0	1	1	0	1	0	0	1	1	1	1	1	0	1	1	1	0	0	0	1	1	1				1	1	1	1	0	0	1	1	1				1
1	0	0	0	1	0	0	0	1	1	0	1	1	0	1	0	1	0	0	0	1	1	0	1	1	1	0	0	1	0	0	0				1	1	1	1	0	1	0	0	0				1
1	0	0	0	1	0	0	1	1	1	0	1	1	0	1	0	1	0	0	1	1	1	0	1	1	1	0	0	1	0	0	1				1	1	1	1	0	1	0	0	1				1
1	0	0	0	1	0	1	0	1	1	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	1	0	0	1	0	1	0				1	1	1	1	0	1	0	1	0				1
1	0	0	0	1	0	1	1	1	1	0	1	1	0	1	0	1	0	1	1	1	1	0	1	1	1	0	0	1	0	1	1				1	1	1	1	0	1	0	1	1				1
1	0	0	0	1	1	0	0	1	1	0	1	1	0	1	0	1	1	0	0	1	1	0	1	1	1	0	0	1	1	0	0				1	1	1	1	0	1	1	0	0				1
1	0	0	0	1	1	0	1	1	1	0	1	1	0	1	0	1	1	0	1	1	1	0	1	1	1	0	0	1	1	0	1				1	1	1	1	0	1	1	0	1				1
1	0	0	0	1	1	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1	1	0	1	1	1	0	0	1	1	1	0				1	1	1	1	0	1	1	1	0				1
1	0	0	0	1	1	1	1	1	1	0	1	1	0	1	0	1	1	1	1	1	1	0	1	1	1	0	0	1	1	1	1				1	1	1	1	0	1	1	1	1				1
1	0	0	1	0	0	0	0	1	1	0	1	1	0	1	1	0	0	0	0	1	1	0	1	1	1	0	1	0	0	0	0	1	1	0	1	1	1	1	1	0	0	0	0	1	1	0	1
1	0	0	1	0	0	0	1	1	1	0	1	1	0	1	1	0	0	0	1	1	1	0	1	1	1	0	1	0	0	0	1	1	1	0	1	1	1	1	1	0	0	0	1	1	1	0	1
1	0	0	1	0	0	1	0	1	1	0	1	1	0	1	1	0	0	1	0	1	1	0	1	1	1	0	1	0	0	1	0	1	1	0	1	1	1	1	1	0	0	1	0	1	1	0	1
1	0	0	1	0	0	1	1	1	1	0	1	1	0	1	1	0	0	1	1	1	1	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1	0	0	1	1	1	1	0	1
1	0	0	1	0	1	0	0	1	1	0	1	1	0	1	1	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	0	1	1	0	1	1	1	1	1	0	1	0	0	1	1	0	1
1	0	0	1	0	1	0	1	1	1	0	1	1	0	1	1	0	1	0	1	1	1	0	1	1	1	0	1	0	1	0	1	1	1	0	1	1	1	1	1	0	1	0	1	1	1	0	1
1	0	0	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1
1	0	0	1	0	1	1	1	1	1	0	1	1	0	1	1	0	1	1	1	1	1	0	1	1	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1	1	1	1	1	0	1
1	0	0	1	1	0	0	0	1	1	0	1	1	0	1	1	1	0	0	0	1	1	0	1	1	1	0	1	1	0	0	0	1	1	0	1	1	1	1	1	1	0	0	0	1	1	0	1
1	0	0	1	1	0	0	1	1	1	0	1	1	0	1	1	1	0	0	1	1	1	0	1	1	1	0	1	1	0	0	1	1	1	0	1	1	1	1	1	1	0	0	1	1	1	0	1
1	0	0	1	1	0	1	0	1	1	0	1	1	0	1	1	1	0	1	0	1	1	0	1	1	1	0	1	1	0	1	0	1	1	0	1	1	1	1	1	1	0	1	0	1	1	0	1
1	0	0	1	1	0	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	0	1	1	1	1	1	1	0	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	1	0	1	1	0	1	1	1	1	0	0	1	1	0	1	1	1	0	1	1	1	0	0	1	1	0	1	1	1	1	1	1	1	0	0	1	1	0	1
1	0	0	1	1	1	0	1	1	1	0	1	1	0	1	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	0	1
1	0	0	1	1	1	1	0	1	1	0	1	1	0	1	1	1	1	1	0	1	1	0	1	1	1	0	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	0	1
1	0	0	1	1	1	1	1	1	1	0	1	1	0	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1

SHEET 2

SHEET 1

32 SECTORS DRIVE Ø											
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
0	0	0	0	0	0	0	0	0	1		
0	0	0	0	0	0	0	1	0	1		
0	0	0	0	0	0	1	0	0	1		
0	0	0	0	0	0	1	1	0	1		
0	0	0	0	0	1	0	0	0	1		
0	0	0	0	0	1	0	1	0	1		
0	0	0	0	0	1	1	0	0	1		
0	0	0	0	0	1	1	1	0	1		
0	0	0	0	1	0	0	0	0	1		
0	0	0	0	1	0	0	1	0	1		
0	0	0	0	1	0	1	0	0	1		
0	0	0	0	1	0	1	1	0	1		
0	0	0	0	1	1	0	0	0	1		
0	0	0	0	1	1	0	1	0	1		
0	0	0	0	1	1	1	0	0	1		
0	0	0	0	1	1	1	1	0	1		
0	0	0	1	0	0	0	0	0	1		
0	0	0	1	0	0	0	1	0	1		
0	0	0	1	0	0	1	0	0	1		
0	0	0	1	0	0	1	1	0	1		
0	0	0	1	0	1	0	0	0	1		
0	0	0	1	0	1	0	1	0	1		
0	0	0	1	0	1	1	0	0	1		
0	0	0	1	0	1	1	1	0	1		
0	0	0	1	1	0	0	0	0	1		
0	0	0	1	1	0	0	1	0	1		
0	0	0	1	1	0	1	0	0	1		
0	0	0	1	1	0	1	1	0	1		
0	0	0	1	1	1	0	0	0	1		
0	0	0	1	1	1	0	1	0	1		
0	0	0	1	1	1	1	0	0	1		
0	0	0	1	1	1	1	1	1	1		

24 SECTORS DRIVE 1											
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
0	0	1	0	0	0	0	0	0	1		
0	0	1	0	0	0	0	1	0	1		
0	0	1	0	0	0	1	0	0	1		
0	0	1	0	0	0	1	1	0	1		
0	0	1	0	0	1	0	0	0	1		
0	0	1	0	0	1	0	1	0	1		
0	0	1	0	0	1	1	0	0	1		
0	0	1	0	0	1	1	1	0	1		
0	0	1	0	1	0	0	0	0	1		
0	0	1	0	1	0	0	1	0	1		
0	0	1	0	1	0	1	0	0	1		
0	0	1	0	1	0	1	1	0	1		
0	0	1	0	1	1	0	0	0	1		
0	0	1	0	1	1	0	1	0	1		
0	0	1	0	1	1	1	0	0	1		
0	0	1	0	1	1	1	1	0	1		
0	0	1	1	0	0	0	0	0	1		
0	0	1	1	0	0	0	1	0	1		
0	0	1	1	0	0	1	0	0	1		
0	0	1	1	0	0	1	1	0	1		
0	0	1	1	0	1	0	0	0	1		
0	0	1	1	0	1	0	1	0	1		
0	0	1	1	0	1	1	0	0	1		
0	0	1	1	1	0	1	1	1	1		
0	0	1	1	1	0	0	0	1	0		
0	0	1	1	1	0	0	1	1	0		
0	0	1	1	1	0	1	0	1	0		
0	0	1	1	1	0	1	1	1	0		
0	0	1	1	1	1	0	0	1	0		
0	0	1	1	1	1	0	1	1	0		
0	0	1	1	1	1	1	0	1	0		
0	0	1	1	1	1	1	1	1	0		

DRIVE 2											
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
0	1	0	0	0	0	0	0		1		
0	1	0	0	0	0	0	1				
0	1	0	0	0	0	1	0				
0	1	0	0	0	0	1	1				
0	1	0	0	0	1	0	0				
0	1	0	0	0	1	0	1				
0	1	0	0	0	1	1	0				
0	1	0	0	0	1	1	1				
0	1	0	0	1	0	0	0				
0	1	0	0	1	0	0	1				
0	1	0	0	1	0	1	0				
0	1	0	0	1	0	1	1				
0	1	0	0	1	1	0	0				
0	1	0	0	1	1	0	1				
0	1	0	0	1	1	1	0				
0	1	0	0	1	1	1	1				
0	1	0	1	0	0	0	0				
0	1	0	1	0	0	0	1				
0	1	0	1	0	0	1	0				
0	1	0	1	0	0	1	1				
0	1	0	1	0	1	0	0				
0	1	0	1	0	1	0	1				
0	1	0	1	0	1	1	0				
0	1	0	1	0	1	1	1				
0	1	0	1	1	0	0	0				
0	1	0	1	1	0	0	1				
0	1	0	1	1	0	1	0				
0	1	0	1	1	0	1	1				
0	1	0	1	1	1	0	0				
0	1	0	1	1	1	0	1				
0	1	0	1	1	1	1	0				
0	1	0	1	1	1	1	1				

DRIVE 3											
ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9			
0	1	1	0	0	0	0	0		1		
0	1	1	0	0	0	0	1				
0	1	1	0	0	0	1	0				
0	1	1	0	0	0	1	1				
0	1	1	0	0	1	0	0				
0	1	1	0	0	1	0	1				
0	1	1	0	0	1	1	0				
0	1	1	0	0	1	1	1				
0	1	1	0	1	0	0	0				
0	1	1	0	1	0	0	1				
0	1	1	0	1	0	1	0				
0	1	1	0	1	0	1	1				
0	1	1	0	1	1	0	0				
0	1	1	0	1	1	0	1				
0	1	1	0	1	1	1	0				
0	1	1	0	1	1	1	1				
0	1	1	1	0	0	0	0				
0	1	1	1	0	0	0	1				
0	1	1	1	0	0	1	0				
0	1	1	1	0	0	1	1				
0	1	1	1	0	1	0	0				
0	1	1	1	0	1	0	1				
0	1	1	1	0	1	1	0				
0	1	1	1	0	1	1	1				
0	1	1	1	1	0	0	0				
0	1	1	1	1	0	0	1				
0	1	1	1	1	0	1	0				
0	1	1	1	1	0	1	1				
0	1	1	1	1	1	0	0				
0	1	1	1	1	1	0	1				
0	1	1	1	1	1	1	0				
0	1	1	1	1	1	1	1				

DRIVE Ø — 32 SECTORS

ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
1	0	0	0	0	0	0	0	1	0		
1	0	0	0	0	0	0	1	1	0		
1	0	0	0	0	0	1	0	1	0		
1	0	0	0	0	0	1	1	1	0		
1	0	0	0	0	1	0	0	1	0		
1	0	0	0	0	1	0	1	1	0		
1	0	0	0	0	1	1	0	1	0		
1	0	0	0	0	1	1	1	1	0		
1	0	0	0	1	0	0	0	1	0		
1	0	0	0	1	0	0	1	1	0		
1	0	0	0	1	0	1	0	1	0		
1	0	0	0	1	0	1	1	1	0		
1	0	0	0	1	1	0	0	1	0		
1	0	0	0	1	1	0	1	1	0		
1	0	0	0	1	1	1	0	1	0		
1	0	0	0	1	1	1	1	1	0		
1	0	0	1	0	0	0	0	1	0		
1	0	0	1	0	0	0	1	1	0		
1	0	0	1	0	0	1	0	1	0		
1	0	0	1	0	0	1	1	1	0		
1	0	0	1	0	1	0	0	1	0		
1	0	0	1	0	1	0	1	1	0		
1	0	0	1	0	1	1	0	1	0		
1	0	0	1	0	1	1	1	1	0		
1	0	0	1	1	0	0	0	1	0		
1	0	0	1	1	0	0	1	1	0		
1	0	0	1	1	0	1	0	1	0		
1	0	0	1	1	0	1	1	1	0		
1	0	0	1	1	1	0	0	1	0		
1	0	0	1	1	1	0	1	1	0		
1	0	0	1	1	1	1	0	1	0		
1	0	0	1	1	1	1	1	1	0		

DRIVE 1 — 24 SECTORS

ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
1	0	1	0	0	0	0	0	1	0		
1	0	1	0	0	0	0	1	1	0		
1	0	1	0	0	0	1	0	1	0		
1	0	1	0	0	0	1	1	1	0		
1	0	1	0	0	1	0	0	1	0		
1	0	1	0	0	1	0	1	1	0		
1	0	1	0	0	1	1	0	1	0		
1	0	1	0	0	1	1	1	1	0		
1	0	1	0	1	0	0	0	1	0		
1	0	1	0	1	0	0	1	1	0		
1	0	1	0	1	0	1	0	1	0		
1	0	1	0	1	0	1	1	1	0		
1	0	1	0	1	1	0	0	1	0		
1	0	1	0	1	1	0	1	1	0		
1	0	1	0	1	1	1	0	1	0		
1	0	1	0	1	1	1	1	1	0		
1	0	1	1	0	0	0	0	1	0		
1	0	1	1	0	0	0	1	1	0		
1	0	1	1	0	0	1	0	1	0		
1	0	1	1	0	0	1	1	1	0		
1	0	1	1	0	1	0	0	1	0		
1	0	1	1	0	1	0	1	1	0		
1	0	1	1	0	1	1	0	1	0		
1	0	1	1	0	1	1	1	1	0		
1	0	1	1	1	0	0	0	1	0		
1	0	1	1	1	0	0	1	1	0		
1	0	1	1	1	0	1	0	1	0		
1	0	1	1	1	0	1	1	1	0		
1	0	1	1	1	1	0	0	1	0		
1	0	1	1	1	1	0	1	1	0		
1	0	1	1	1	1	1	0	1	0		
1	0	1	1	1	1	1	1	1	0		

DRIVE 2

ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
1	1	0	0	0	0	0	0	1	0		
1	1	0	0	0	0	0	1	1	0		
1	1	0	0	0	0	1	0	1	0		
1	1	0	0	0	0	1	1	1	0		
1	1	0	0	0	1	0	0	1	0		
1	1	0	0	0	1	0	1	1	0		
1	1	0	0	0	1	1	0	1	0		
1	1	0	0	0	1	1	1	1	0		
1	1	0	0	1	0	0	0	1	0		
1	1	0	0	1	0	0	1	1	0		
1	1	0	0	1	0	1	0	1	0		
1	1	0	0	1	0	1	1	1	0		
1	1	0	0	1	1	0	0	1	0		
1	1	0	0	1	1	0	1	1	0		
1	1	0	0	1	1	1	0	1	0		
1	1	0	0	1	1	1	1	1	0		
1	1	0	1	0	0	0	0	1	0		
1	1	0	1	0	0	0	1	1	0		
1	1	0	1	0	0	1	0	1	0		
1	1	0	1	0	0	1	1	1	0		
1	1	0	1	0	1	0	0	1	0		
1	1	0	1	0	1	0	1	1	0		
1	1	0	1	0	1	1	0	1	0		
1	1	0	1	0	1	1	1	1	0		
1	1	0	1	1	0	0	0	1	0		
1	1	0	1	1	0	0	1	1	0		
1	1	0	1	1	0	1	0	1	0		
1	1	0	1	1	0	1	1	1	0		
1	1	0	1	1	1	0	0	1	0		
1	1	0	1	1	1	0	1	1	0		
1	1	0	1	1	1	1	0	1	0		
1	1	0	1	1	1	1	1	1	0		

DRIVE 3

ILL H	USB	USA	SØ	S1	S2	S3	S4	LAST S	ILL S		
H	G	F	E	D	C	B	A	4	3	2	1
15	1	2	3	4	7	6	5	9	10	11	12
1	1	1	0	0	0	0	0	1	0		
1	1	1	0	0	0	0	1	1	0		
1	1	1	0	0	0	1	0	1	0		
1	1	1	0	0	0	1	1	1	0		
1	1	1	0	0	1	0	0	1	0		
1	1	1	0	0	1	0	1	1	0		
1	1	1	0	0	1	1	0	1	0		
1	1	1	0	0	1	1	1	1	0		
1	1	1	0	1	0	0	0	1	0		
1	1	1	0	1	0	0	1	1	0		
1	1	1	0	1	0	1	0	1	0		
1	1	1	0	1	0	1	1	1	0		
1	1	1	0	1	1	0	0	1	0		
1	1	1	0	1	1	0	1	1	0		
1	1	1	0	1	1	1	0	1	0		
1	1	1	0	1	1	1	1	1	0		
1	1	1	1	0	0	0	0	1	0		
1	1	1	1	0	0	0	1	1	0		
1	1	1	1	0	0	1	0	1	0		
1	1	1	1	0	0	1	1	1	0		
1	1	1	1	0	1	0	0	1	0		
1	1	1	1	0	1	0	1	1	0		
1	1	1	1	0	1	1	0	1	0		
1	1	1	1	0	1	1	1	1	0		
1	1	1	1	1	0	0	0	1	0		
1	1	1	1	1	0	0	1	1	0		
1	1	1	1	1	0	1	0	1	0		
1	1	1	1	1	0	1	1	1	0		
1	1	1	1	1	1	0	0	1	0		
1	1	1	1	1	1	0	1	1	0		
1	1	1	1	1	1	1	0	1	0		
1	1	1	1	1	1	1	1	1	0		

SHEET 2

MANUAL TITLE 700 Disc Controller User Manual

PUBLICATION NO. HM-121-0012 REVISION A

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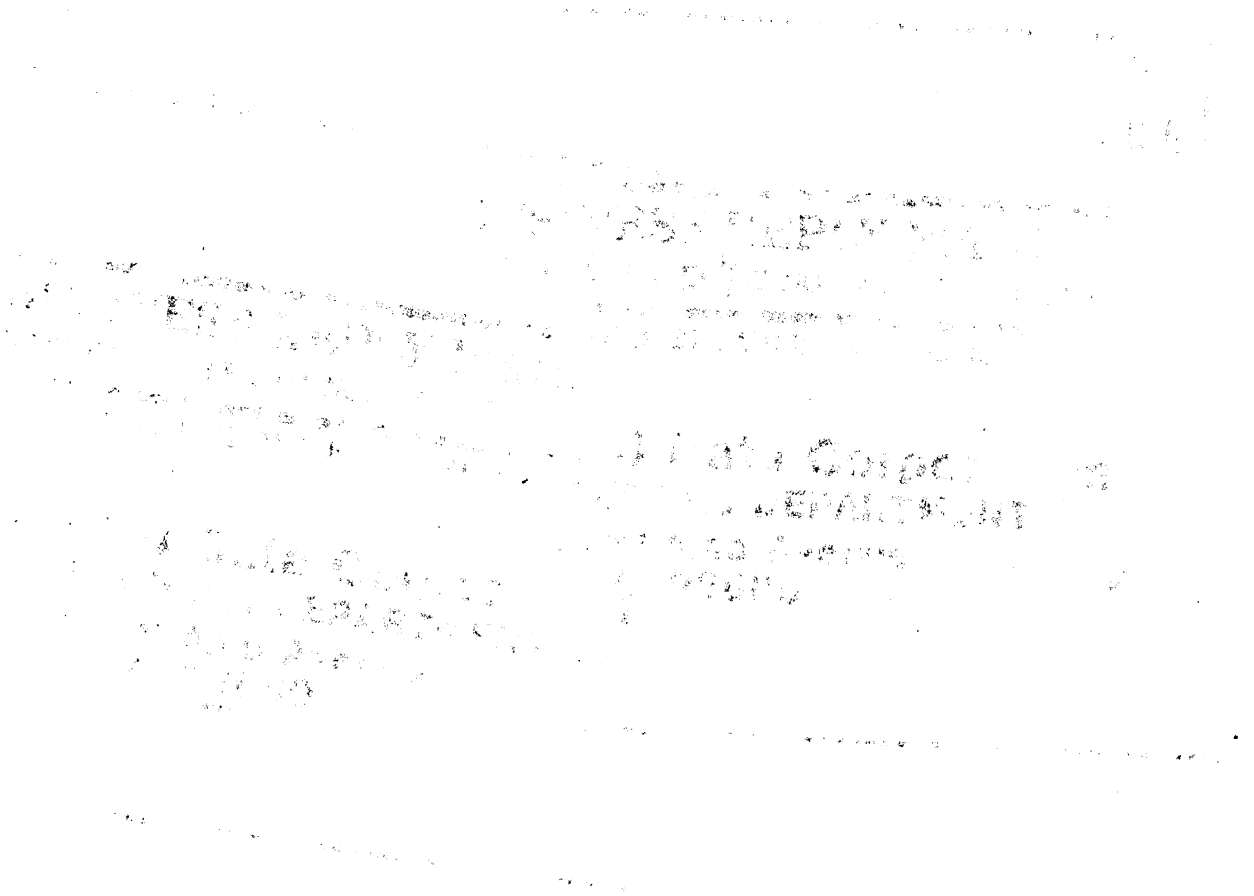

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