

0001 HIUT MACRO REV 06.30 00132153 12/22/78

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: NAME: BASICIOT.TX PART NUMBER: 097-001133
: DESCRIPTION: BASIC INPUT / OUTPUT TEST
: REVISION HISTORY:
: REV. DATE
: 00 12/29/78
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NY Basic I/O

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I. GOAL
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PROVIDE AN ADEQUATE TEST OF RELIABILITY OF THE INPUT/OUTPUT INSTRUCTIONS AND DATA CHANNEL OPERATION. THE PROGRAM SHOULD BE ABLE TO RUN ON ALL COMPUTER TYPES.

THE IUT.SK PROGRAM ALSO INCLUDES A REAL TIME CLOCK EXERCISER.

II. PROGRAM DESCRIPTION
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THE 'INPUT/OUTPUT TEST' PROGRAM (IOT.SK) WILL PERFORM TESTS ON ALL THE I/O INSTRUCTIONS BY USING A MULTIMODE I/O TESTER BOARD DEVELOPED BY TEST EQUIPMENT DESIGN. THE ALGORITHMS DESIGNED FOR THIS PROGRAM ARE BASED ON A SPECIFICATION OF THE I/O TESTER, DRAWING NUMBER 202-000-103, REV. EE. SPECIFIC QUESTIONS ON THE SPECIFICATION CAN BE FORWARDED TO HARRY WHITTEMORE, X5975, MS. B-55, TEST EQUIPMENT DESIGN.

BEFORE RUNNING BASICIOT, THE MULTIMODE I/O TESTER BOARD MUST BE IN PLACE, ALONG WITH THE NECESSARY INTP AND OCHP JUMPERS.

WHEN RUNNING IN MANUAL MODE, THE USER MUST FIRST ENTER A KEY DENOTING WHAT COMPUTER TYPE THE PROGRAM IS RUNNING ON.

PROGRAM EXECUTION TIME IS APPROXIMATELY 25-35 SECONDS.

ON THE REAL TIME CLOCK EXERCISER, LOOP COUNT VARIATIONS DUE TO THE MEMORY REFRESH CYCLE AND THE INDERTIMINATE NATURE OF THE PREFETCH PROCESSOR MAY CAUSE AN INTERMITTENT "RTC FREQUENCY TEST FAILURE". THIS SHOULD BE IGNORED UNLESS THE MESSAGE APPEARS FOR THE MAJORITY OF THE PASSES (IN WHICH CASE IT SHOULD BE TREATED AS AN ACTUAL RTC FREQUENCY TEST FAILURE).

THE PROGRAM WILL TEST THE FOLLOWING ITEMS IN THE FOLLOWING ORDER:

1. DATA OUT, DATA IN INSTRUCTIONS' PULSE VERIFICATION- IS THE CORRECT PULSE ASSERTED ON THE I/O BUS?
2. DATA OUT, DATA IN INSTRUCTIONS' DATA PATH- DO THE INSTRUCTIONS PROPERLY LOAD/READ THE CORRECT REGISTER ON THE I/O TESTER BOARD?
3. DATA OUT, DATA IN, & NIO INSTRUCTIONS' BUSY & DONE OPERATIONS- VERIFY THAT THE 'S', 'C', AND 'P' SUFFIXES CORRECTLY ASSERT THE 'STRT', 'CLR', AND 'IOPLS' I/O BUS SIGNALS, RESPECTIVELY.
4. BUSY & DONE SKIP INSTRUCTIONS- ASSERT OR CLEAR THE SELB AND SELD INSTRUCTIONS TO TEST THE SKP- I/O INSTRUCTIONS.
5. IORST- SHOULD CLEAR ALL REGISTERS.

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4. DEVICE SELECT TEST- ISSUE AN IORST TO CLEAN ALL DEVICES' BUSY FLAGS. SET THE BUSY FLAG ON THE I/O TESTER (DEVICE CODE 00). EXECUTE SUCCESSIVE SKIP-ON-BUSY-FLAG INSTRUCTIONS FOR DEVICE CODES 2-76 (1 AND 77 WOULD CAUSE TROUBLE). IF THERE ARE ANY OTHER BUSY FLAGS SET, THEN THERE IS AN ERROR ON THE DEVICE CODE LINES.
7. MSKO- CHECK THAT THE MSKO PULSE WAS SENT ON THE I/O BUS.
8. INTA- CHECK THAT THE INTA PULSE WAS SENT ON THE I/O BUS. THE I/O TESTER BOARD PROVIDES AN ADDITIONAL TEST OF INTA. SPECIFICALLY, IT HEADS THE DATA REGISTER IN OLD MODE.
9. VERIFY DATA CHANNEL OUT (DCHO) AND DATA CHANNEL IN (DCMI) I/O PULSES.
10. PROGRAM INTERRUPT COUNTER TEST- AN INTERRUPT CAN BE MADE TO OCCUR AS A FUNCTION OF THE NUMBER OF REQUEST ENABLE PULSES (AS SPECIFIED IN THE MDENH CTR IN THE FUNCTION REGISTER) AND AS A FUNCTION OF THE COMPUTER TYPE. FOR THIS TEST, START THE FUNCTION REGISTER'S PROGRAMMED INTERRUPT COUNTER, AND START A LOOP COUNTER INCREMENTING. WHEN THE PROGRAM INTERRUPT OCCURS, THE LOOP COUNTER SHOULD BE WITHIN A YET TO BE DETERMINED RANGE OF A COMPUTER TYPE-SPECIFIC CONSTANT. THE CONSTANT AND ITS RANGE WILL BE DETERMINED THROUGH EXPERIMENTATION. THIS TEST IS RUN ONLY IN DTUS MANUAL MODE.
11. DATA CHANNEL INPUT TEST- IN NEW MODE, VARY THE MEMORY DATA BUFFER ADDRESS (DBA), NUMBER OF WORDS TRANSFERRED PER DATA CHANNEL OUT CALL (I.E., THE DATA CHANNEL RANGE, DCHR), THE NUMBER OF REQUEST ENABLE PULSES BETWEEN TRANSFERRED WORDS (REQC, REQUEST ENABLE COUNT), AND THE SEED FOR THE RANDOM NUMBER GENERATOR (SEED). IN ALL CASES, THE NUMBERS INPUTTED FROM THE TESTER BOARD SHOULD EQUAL THE NUMBERS GENERATED BY AN EQUIVALENT SOFTWARE RANDOM NUMBER GENERATOR.
12. DATA CHANNEL OUTPUT TEST- IN NEW MODE, VARY THE SAME VARIABLES. EXCEPT THAT A BUFFER OF NUMBERS FROM MEMORY WILL BE INPUTTED INTO THE TESTER BOARD. THE NEW NUMBER IN THE DATA REGISTER AFTER EACH WORD INPUTTED WILL BE THE PREVIOUS VALUE OF THE DATA REGISTER EXCLUSIVE ORRED WITH THE INPUTTED NUMBER (THE ORIGINAL VALUE OF THE DATA REGISTER BEING 0). AT THE END OF THE TRANSFER, IF THE EXPECTED DATA IS NOT IN THE DATA REGISTER, OR THE ADDRESS REGISTER \neq DBA+(DCHR*1)+8, THEN AN ERROR OCCURRED.
13. REAL TIME CLOCK EXERCISER- TEST THE 10, 100, AND 1000 HZ FREQUENCIES AGAINST THE 60 HZ FREQUENCY FOR REASONABLE ACCURACY. USES INTERRUPTS, LOOP COUNTS, AND TIMEOUT ERROR CHECKING. SEE PARAGRAPH ABOVE REGARDING RTC FREQUENCY TEST FAILURES.

.ENDC
.EJEC

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; NAME: MASIC10T.SW PART NUMBER: 098-001514
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; DESCRIPTION: MASIC INPUT / OUTPUT TEST
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; REVISION HISTORY:
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; REV. DATE
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; 00 12/29/78
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