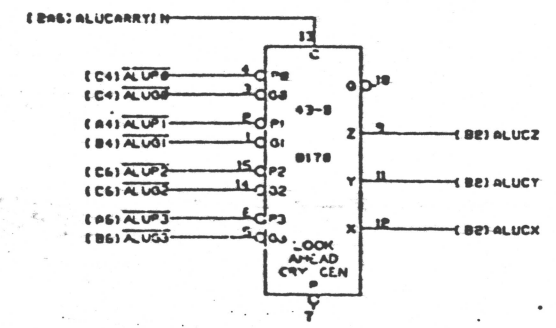
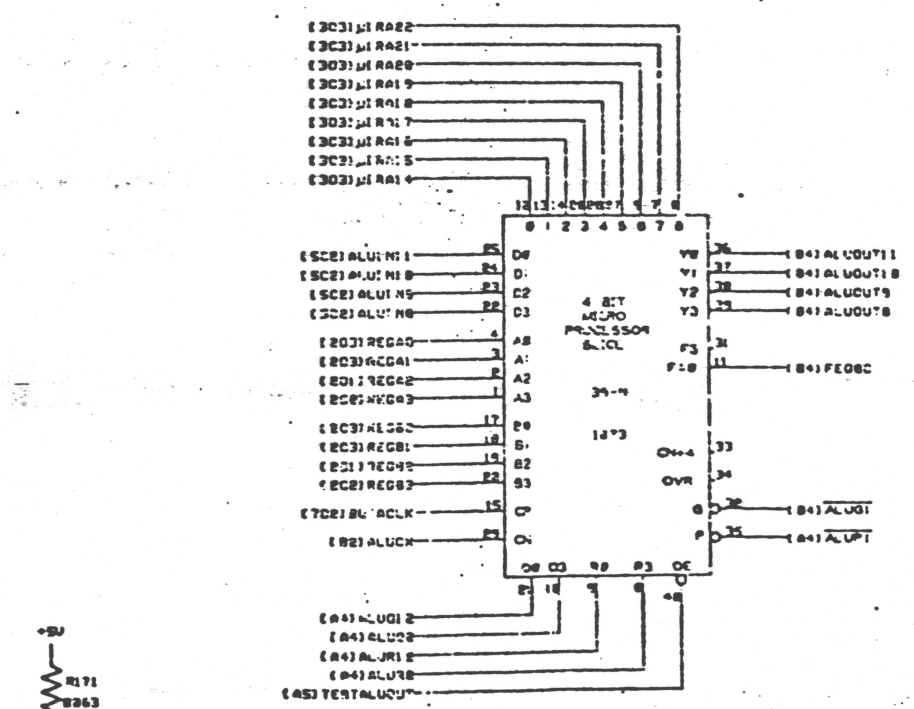
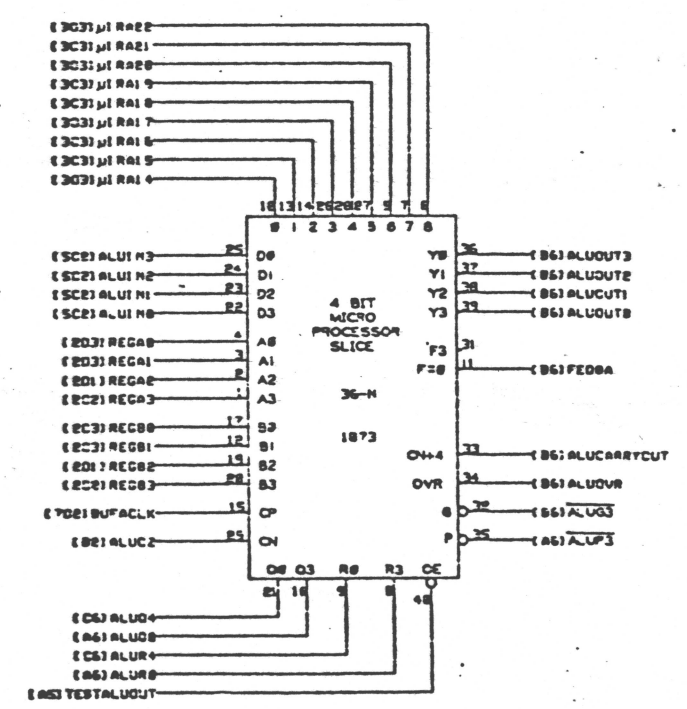
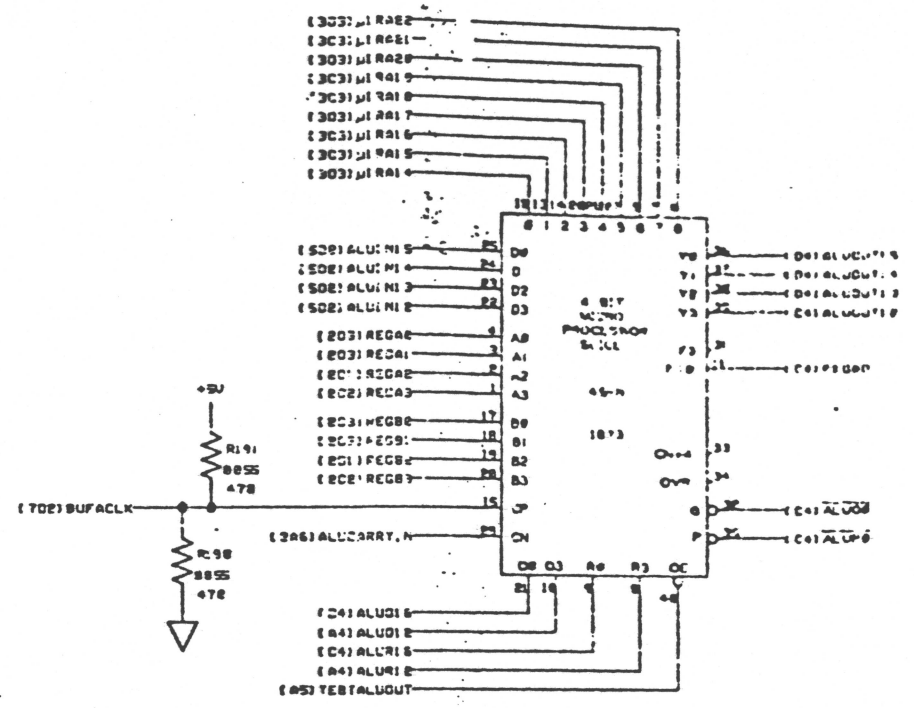
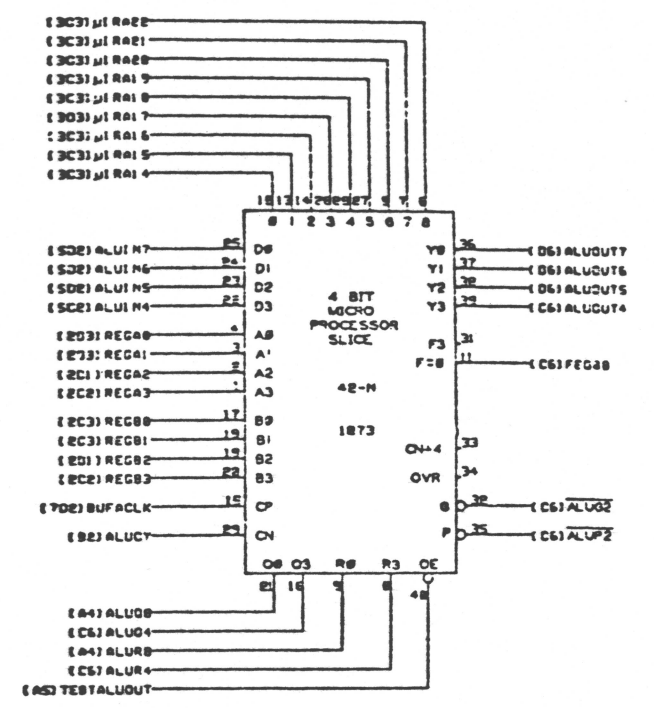


DO NOT SCALE DIMENSIONS AND  
 DIMENSIONS TO BE SHOWN TO THE NEAREST 0.001"  
 UNLESS OTHERWISE SPECIFIED

REV	DESCRIPTION	DATE	APP BY
00	MCU PER ECO F023		
01	PER ECO F023		
02	PER ECO F064		
03	PER ECO G700		
04	PER ECO G703		
05	PER ECO 9622		
06	PER ECO 2-95C		
07	PER ECO G723 DIG. CLK		



SPARE GATES

0799	03-J	02
0797	03-M	01
0365	05-W	01
0700	05A6	01
1000	07-J	02
0159	07A4	03
0627	09-B	01
0630	09-F	01
0537	09-S	01
0060	09A4	02
0070	09A4	01
1064	11A4	01
1000	13A4	02
0133	15-N	02
0366	15A4	02
1150	15A4	01
0417	17A4	02
0175	19-W	01
0537	21A4	01
0300	21A4	01
0797	27-F	01
0365	29-S	02
0307	33-B	01
1020	33-J	01
0575	36-F	01
0575	40-F	01
0417	41-B	01
0175	43-W	01

CHART 1

	UNTESTED	TESTED
00M	005-12410	005-12411
100M	005-12412	005-12413
200M	005-12414	005-12415

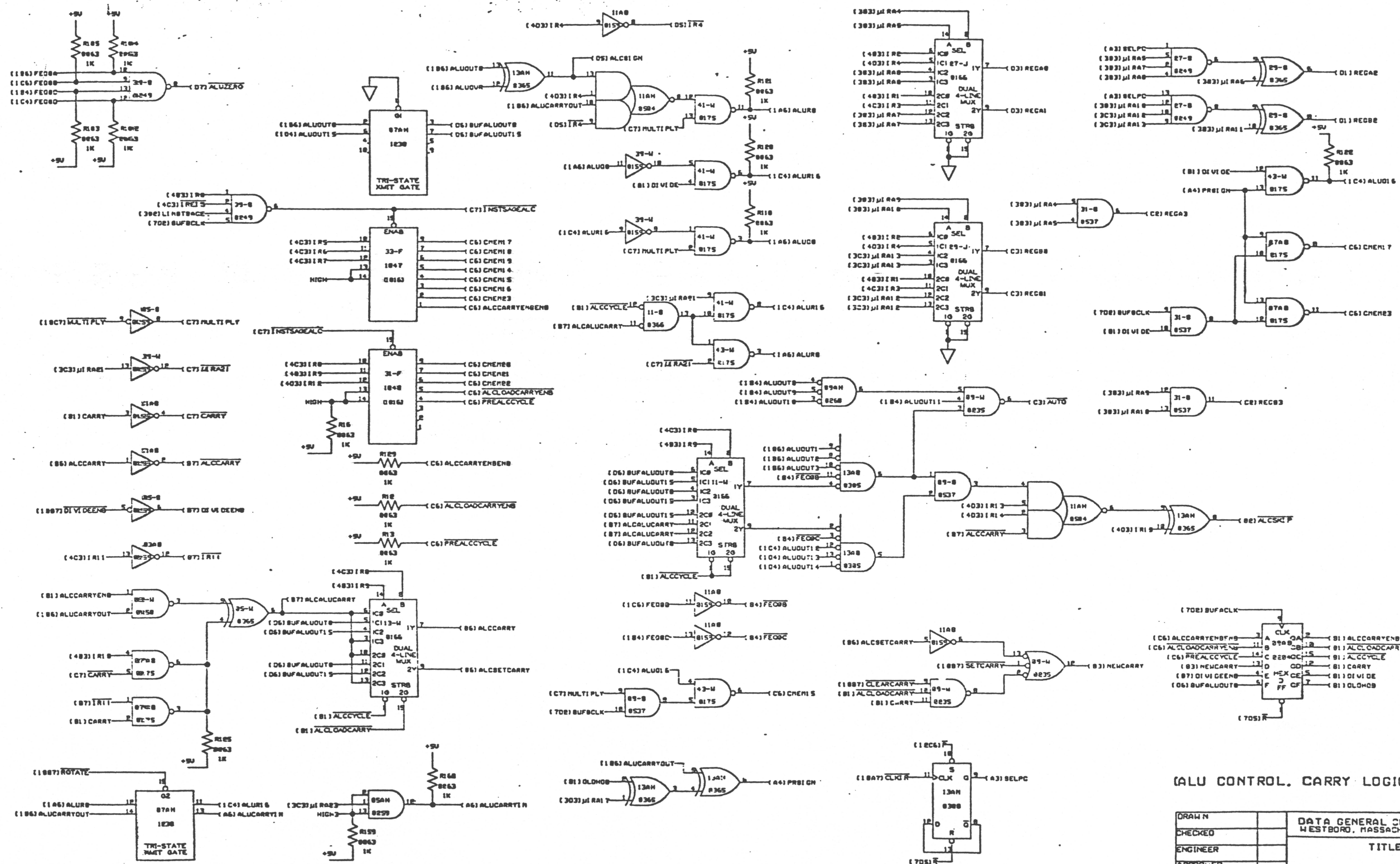
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ANTWORK: 107 1307	DRAWN	DATE	DATA GENERAL CORPORATION WESTBORO, MASSACHUSETTS 01581
ANTWORK VS SCHEMATIC	CHECKED	10/6/79	TITLE
REV: SCHEMATIC REV: 1	ENGINEER	10/11/79	NOVA 4/C CPU
00 00 00 00 00 00	APPROVED	10/17/79	001001600
01 07	FIRST USED ON		SEE CHART 1
	SIZE CODE	DRAWING NUMBER	REV

See page 3 for options

SMALL PRINT AS SUPPLIED BY THE MANUFACTURER OR IN ACCORDANCE WITH THE DATA SHEET FOR THE MANUFACTURER'S SPECIFICATIONS.

REV. DESCRIPTION DATE BY



(ALU CONTROL CARRY LOGIC)

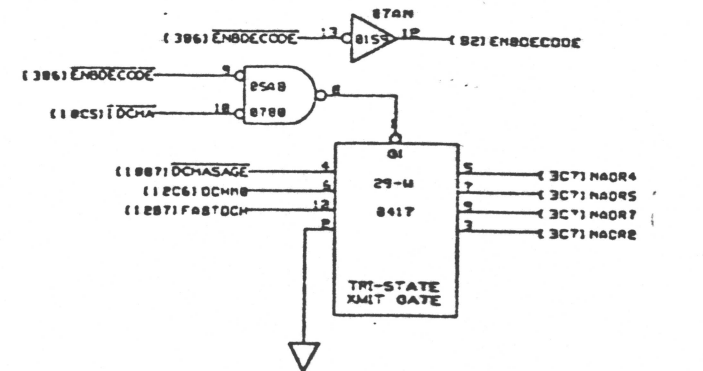
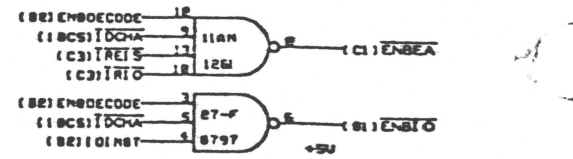
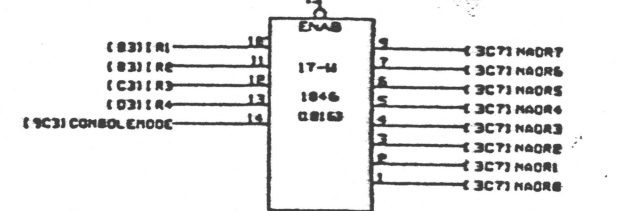
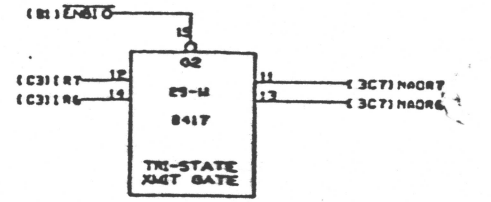
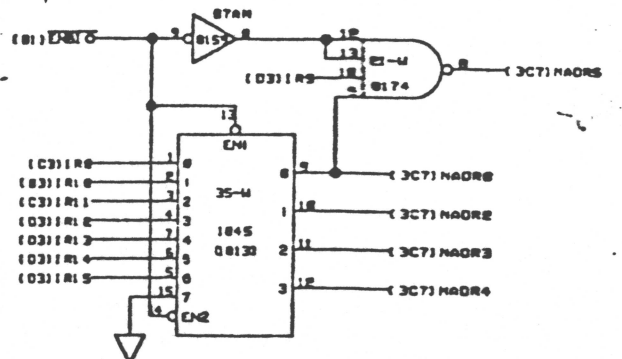
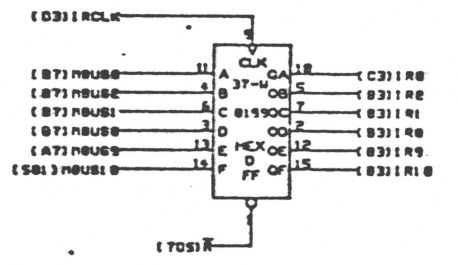
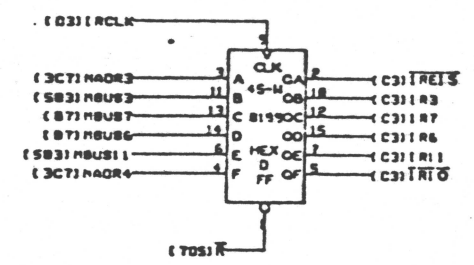
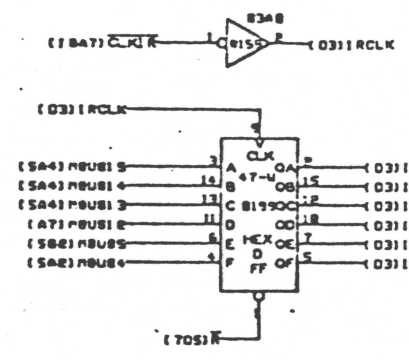
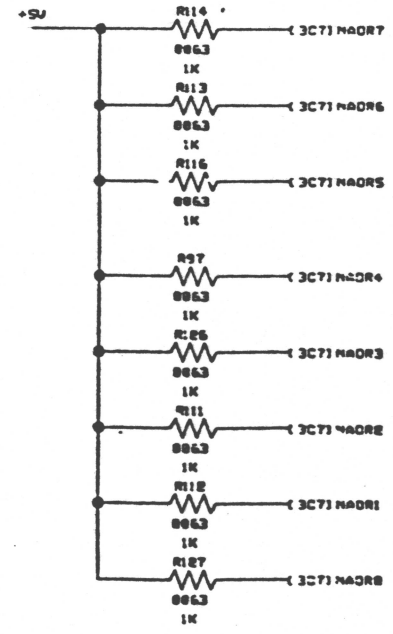
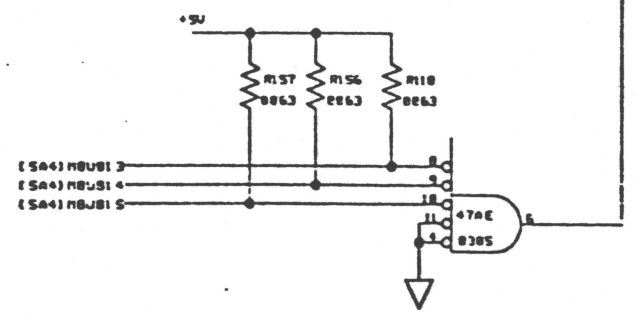
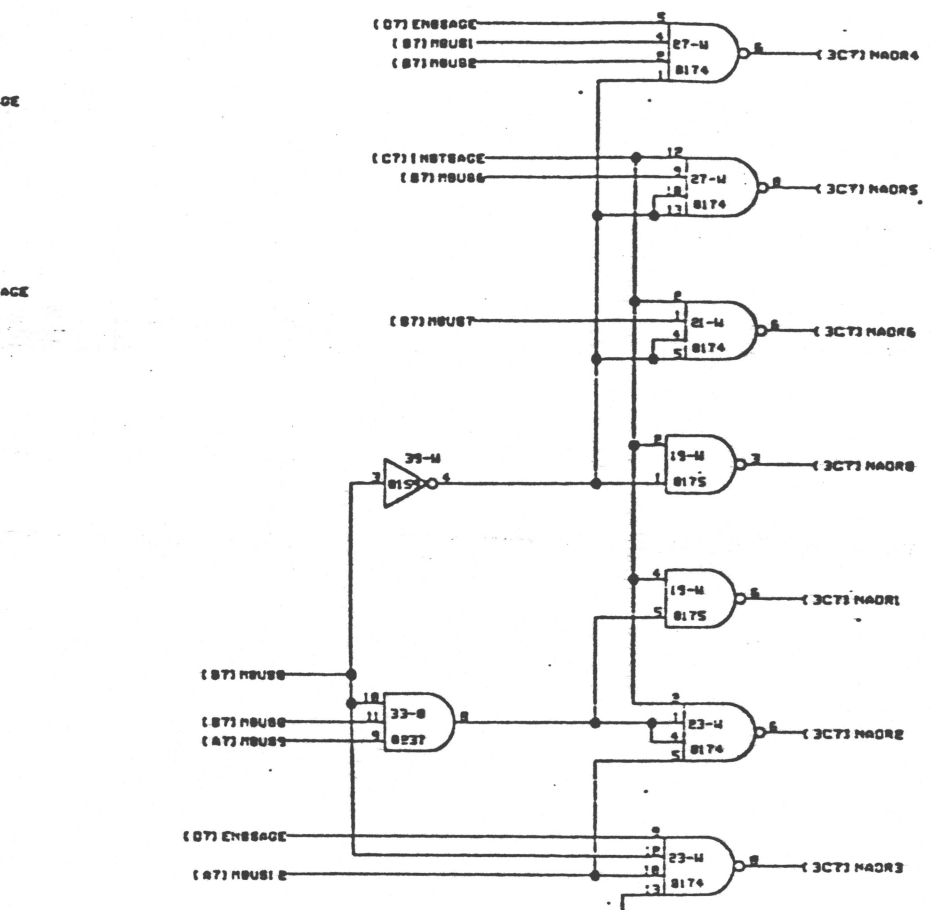
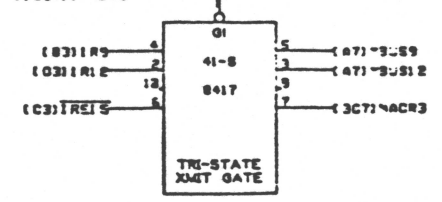
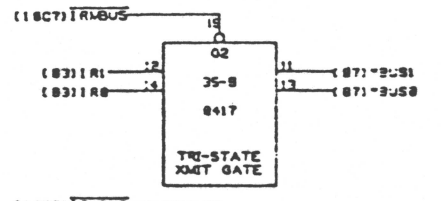
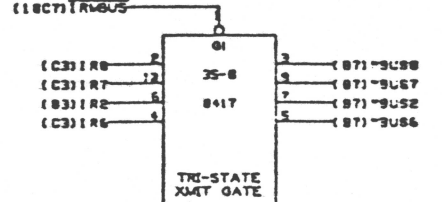
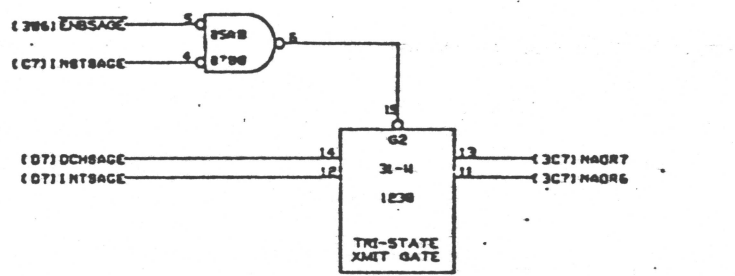
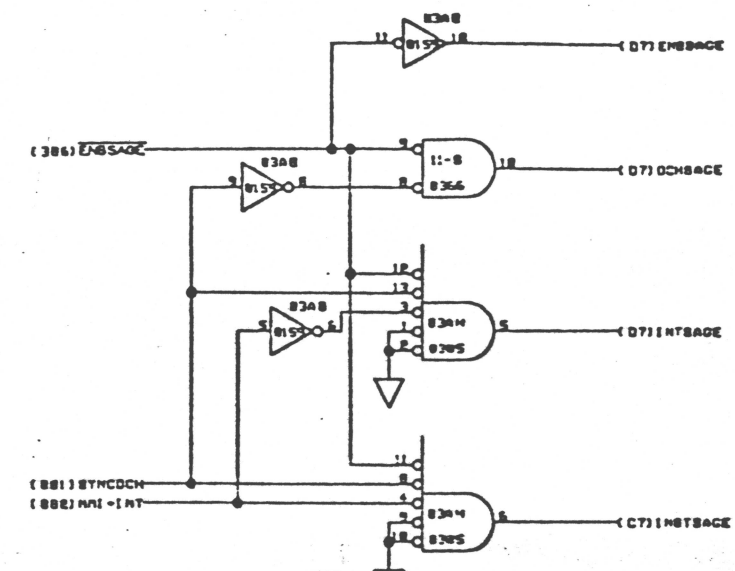
DRAWN		DATA GENERAL CORPORATION
CHECKED		WESTBORO, MASSACHUSETTS 01581
ENGINEER		TITLE
APPROVED		NOVA 4/C
FIRST USED ON		SIZE CODE DRAWING NUMBER
		001001600

474



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REV DESCRIPTION DFTS APP BY DT



(SAGE, DECODE, IR)

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ENGINEER	TITLE
APPROVED	NOVA 4/5
FIRST USED ON	SIZE CODE DRAWING NUMBER

001001600

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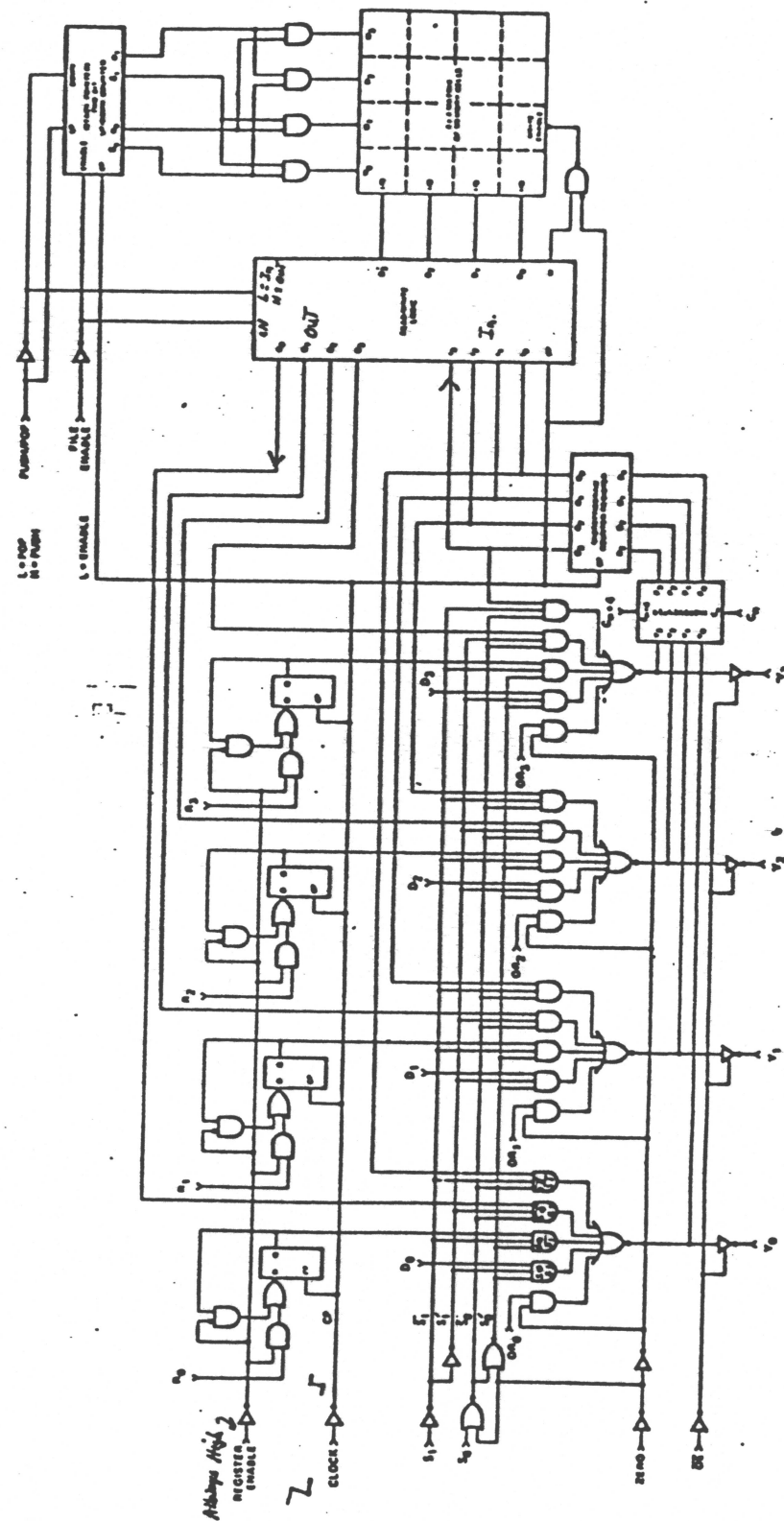
7 6 5 4 3 2 1 SHEET AND 2



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100001074  
(Continued)

MICROPROGRAM SEQUENCER BLOCK DIAGRAM



100001074  
(Continued)

ADDRESS SELECTION

OCTAL	S <sub>1</sub>	S <sub>0</sub>	SOURCE FOR Y OUTPUTS	SYMBOL
0	L	L	Microprogram Counter	μPC
1	L	H	Register	REG
2	H	L	Push-Pop stack	STK0
3	H	H	Direct inputs	D <sub>i</sub>

OUTPUT CONTROL

O/E <sub>1</sub>	ZERO	O/E	Y <sub>i</sub>
X	X	H	Z
X	L	L	L
H	H	L	H
L	H	L	Source selected by S <sub>0</sub> S <sub>1</sub>

Z = High Impedance

SYNCHRONOUS STACK CONTROL

F <sub>E</sub>	PUP	PUSH-POP STACK CHANGE
H	X	No change
L	H	Increment stack pointer, then push current PC onto STK0
L	L	Pop stack (decrement stack pointer)

H = High  
L = Low  
X = Don't Care

OUTPUT AND INTERNAL NEXT-CYCLE REGISTER STATES

CYCLE	S <sub>1</sub> , S <sub>0</sub> , F <sub>E</sub> , PUP	Internal								COMMENT	PRINCIPLE USE
		μPC	REG	STK0	STK1	STK2	STK3	Y <sub>OUT</sub>			
N N+1	0 0 0 0 -	J J+1	K K	R <sub>a</sub> R <sub>b</sub>	R <sub>b</sub> R <sub>c</sub>	R <sub>c</sub> R <sub>d</sub>	R <sub>d</sub> R <sub>a</sub>	J -	Pop Stack	End Loop	
N N+1	0 0 0 1 -	J J+1	K K	R <sub>a</sub> J	R <sub>b</sub> R <sub>a</sub>	R <sub>c</sub> R <sub>b</sub>	R <sub>d</sub> R <sub>c</sub>	J -	Push μPC	Set-up Loop	
N N+1	0 0 1 X -	J J+1	K K	R <sub>a</sub> R <sub>a</sub>	R <sub>b</sub> R <sub>b</sub>	R <sub>c</sub> R <sub>c</sub>	R <sub>d</sub> R <sub>d</sub>	J -	Continue	Continue	
N N+1	0 1 0 0 -	J K+1	K K	R <sub>a</sub> R <sub>b</sub>	R <sub>b</sub> R <sub>c</sub>	R <sub>c</sub> R <sub>d</sub>	R <sub>d</sub> R <sub>a</sub>	K -	Pop Stack; Use AR for Address	End Loop	
N N+1	0 1 0 1 -	J K+1	K K	R <sub>a</sub> J	R <sub>b</sub> R <sub>a</sub>	R <sub>c</sub> R <sub>b</sub>	R <sub>d</sub> R <sub>c</sub>	K -	Push μPC; Jump to Address in AR	JSR AR	
N N+1	0 1 1 X -	J K+1	K K	R <sub>a</sub> R <sub>a</sub>	R <sub>b</sub> R <sub>b</sub>	R <sub>c</sub> R <sub>c</sub>	R <sub>d</sub> R <sub>d</sub>	K -	Jump to Address in AR	JMP AR	
N N+1	1 0 0 0 -	J R <sub>a</sub> +1	K K	R <sub>a</sub> R <sub>b</sub>	R <sub>b</sub> R <sub>c</sub>	R <sub>c</sub> R <sub>d</sub>	R <sub>d</sub> R <sub>a</sub>	R <sub>a</sub> -	Jump to Address in STK0; Pop Stack	RTS	
N N+1	1 0 0 1 -	J R <sub>a</sub> +1	K K	R <sub>a</sub> J	R <sub>b</sub> R <sub>a</sub>	R <sub>c</sub> R <sub>b</sub>	R <sub>d</sub> R <sub>c</sub>	R <sub>a</sub> -	Jump to Address in STK0; Push μPC		
N N+1	1 0 1 X -	J R <sub>a</sub> +1	K K	R <sub>a</sub> R <sub>a</sub>	R <sub>b</sub> R <sub>b</sub>	R <sub>c</sub> R <sub>c</sub>	R <sub>d</sub> R <sub>d</sub>	R <sub>a</sub> -	Jump to Address in STK0	Stack Ref (Loop)	
N N+1	1 1 0 0 -	J D+1	K K	R <sub>a</sub> R <sub>b</sub>	R <sub>b</sub> R <sub>c</sub>	R <sub>c</sub> R <sub>d</sub>	R <sub>d</sub> R <sub>a</sub>	D -	Pop Stack; Jump to Address on D	End Loop	
N N+1	1 1 0 1 -	J D+1	K K	R <sub>a</sub> J	R <sub>b</sub> R <sub>a</sub>	R <sub>c</sub> R <sub>b</sub>	R <sub>d</sub> R <sub>c</sub>	D -	Jump to Address on D; Push μPC	JSR D	
N N+1	1 1 1 X -	J D+1	K K	R <sub>a</sub> R <sub>a</sub>	R <sub>b</sub> R <sub>b</sub>	R <sub>c</sub> R <sub>c</sub>	R <sub>d</sub> R <sub>d</sub>	D -	Jump to Address on D	JMP D	

X = Don't care, 0 = LOW, 1 = HIGH, Assume C<sub>n</sub> = HIGH  
Note: STK0 is the location addressed by the stack pointer.

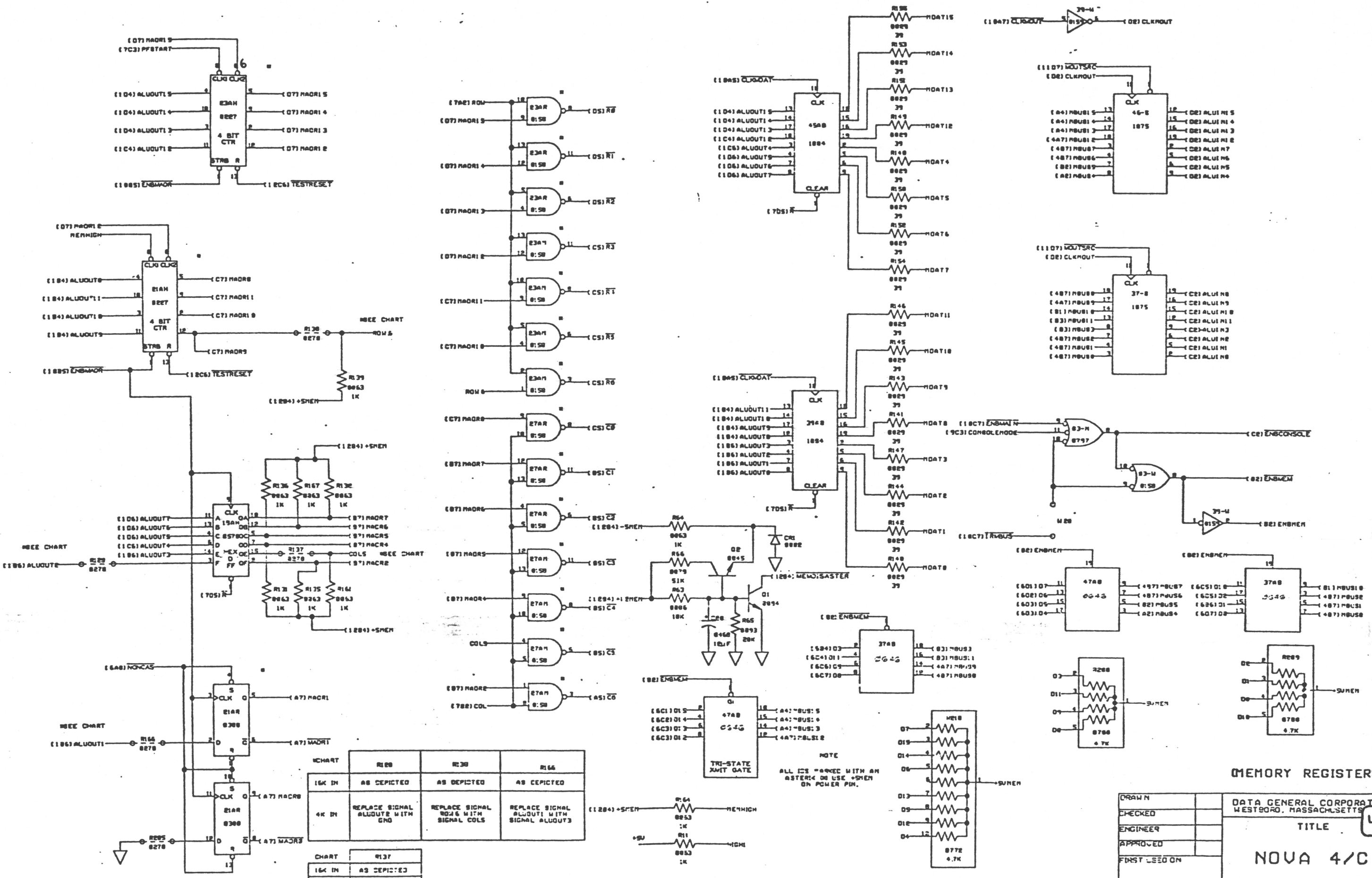


CHART	R188	R230	R166
16K IN	AS DEPICTED	AS DEPICTED	AS DEPICTED
4K IN	REPLACE SIGNAL ALUOUT1 WITH GND	REPLACE SIGNAL ROW6 WITH SIGNAL COLS	REPLACE SIGNAL ALUOUT3 WITH SIGNAL ALUOUT3

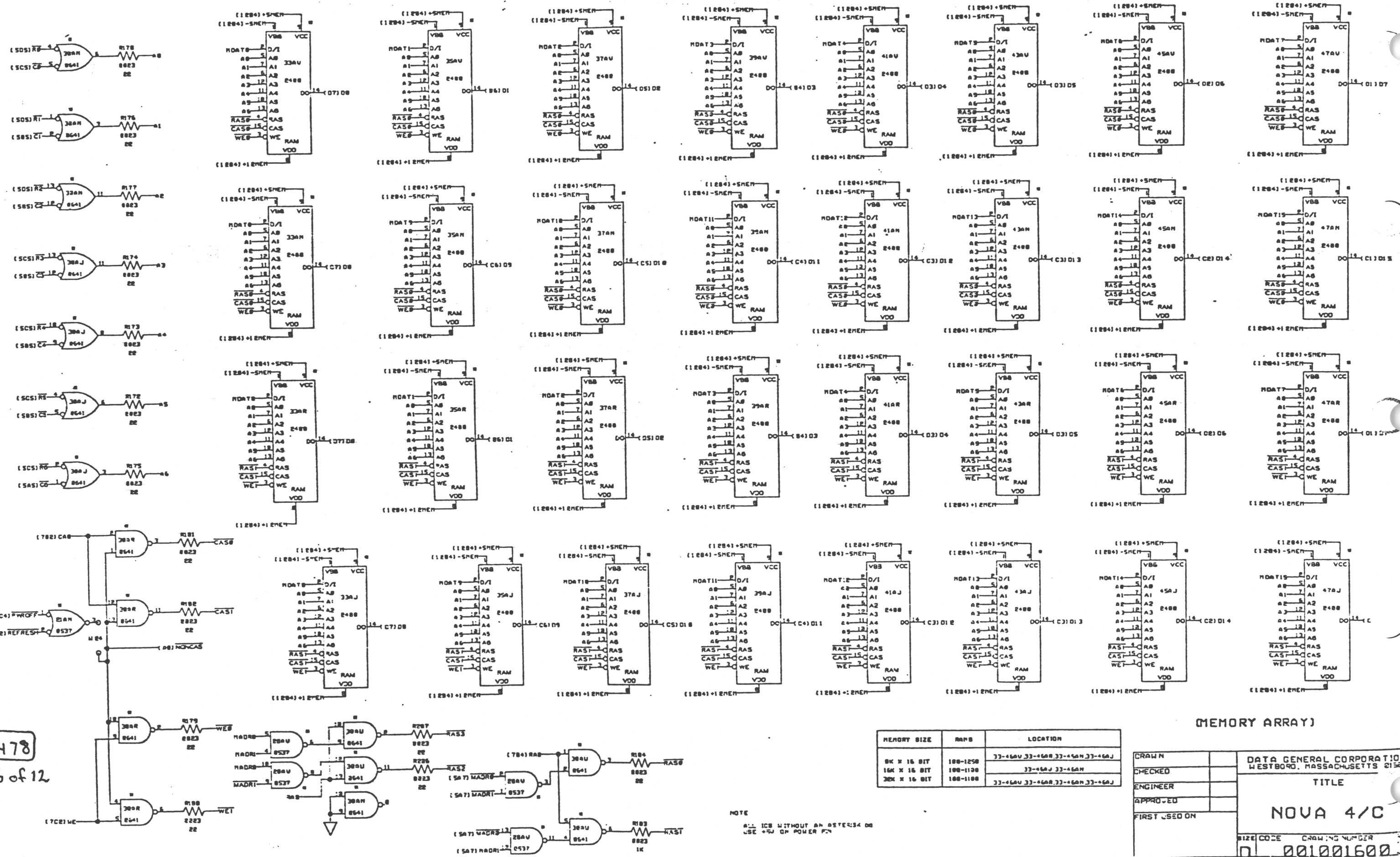
CHART	R137
16K IN	AS DEPICTED
4K IN	REMOVED

NOTE: ALL IC'S \*MAY\* BE USED WITH AN ASTERISK ON POWER PIN.

MEMORY REGISTERS

DRAWN		DATA GENERAL CORPORATION WESTBORO, MASSACHUSETTS
CHECKED		TITLE
ENGINEER		NOVA 4/C
APPROVED		SIZE CODE
FIRST REVISION		DRAWING NUMBER

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MEMORY SIZE	RAMP	LOCATION
8K X 16 BIT	100-1250	33-660J 33-660J 33-660J 33-660J
16K X 16 BIT	100-1100	33-660J 33-660J
32K X 16 BIT	100-1100	33-660J 33-660J 33-660J 33-660J

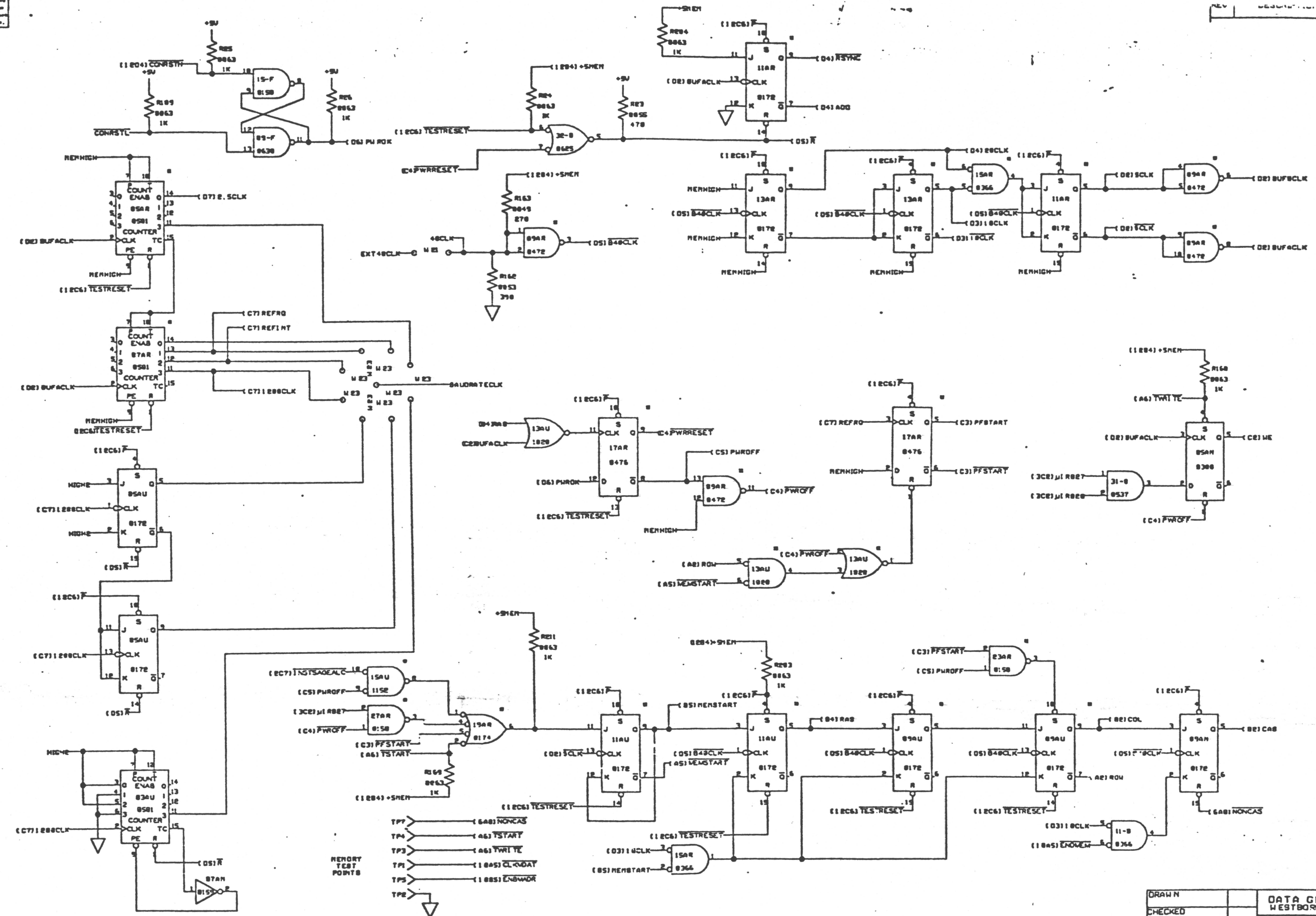
NOTE  
ALL IC'S WITHOUT AN IDENTIFIER ARE  
USE +5V OR POWER PIN

MEMORY ARRAY

CRAWN		DATA GENERAL CORPORATION WESTBORO, MASSACHUSETTS 01581
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		
TITLE		NOVA 4/C
SIZE	CODE	
0	001001600	



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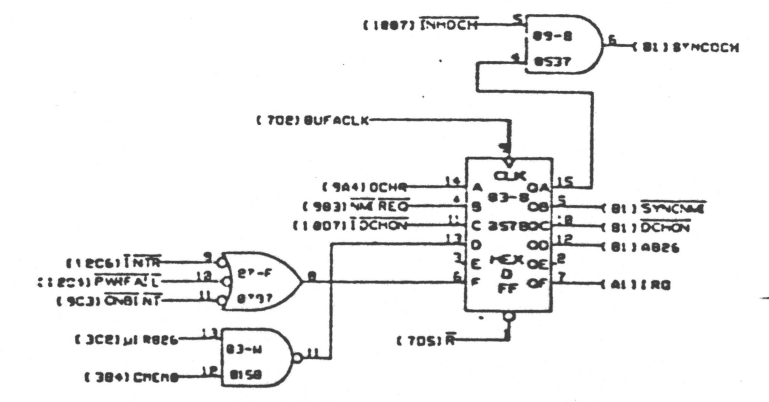
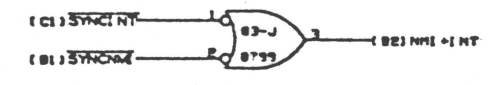
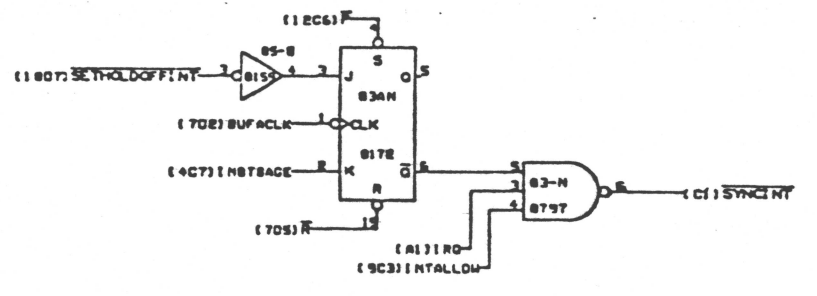
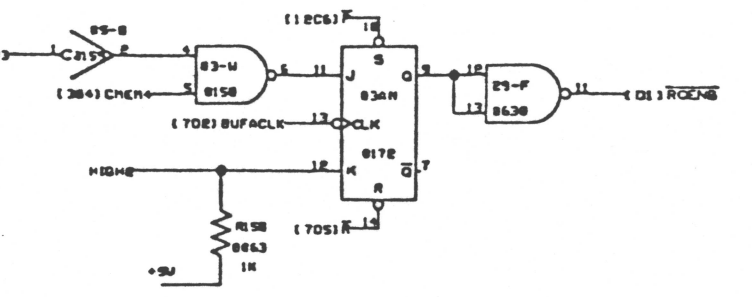
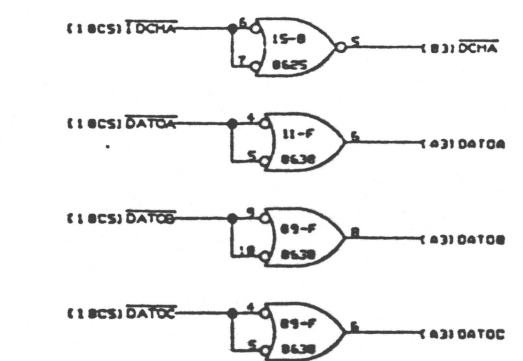
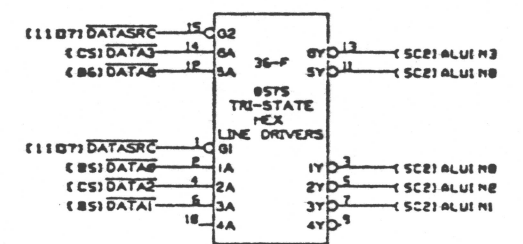
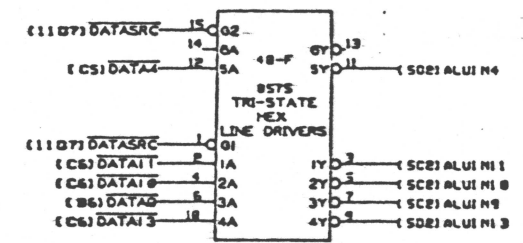
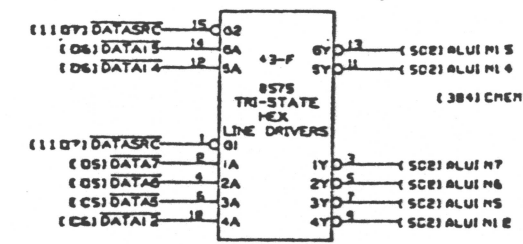
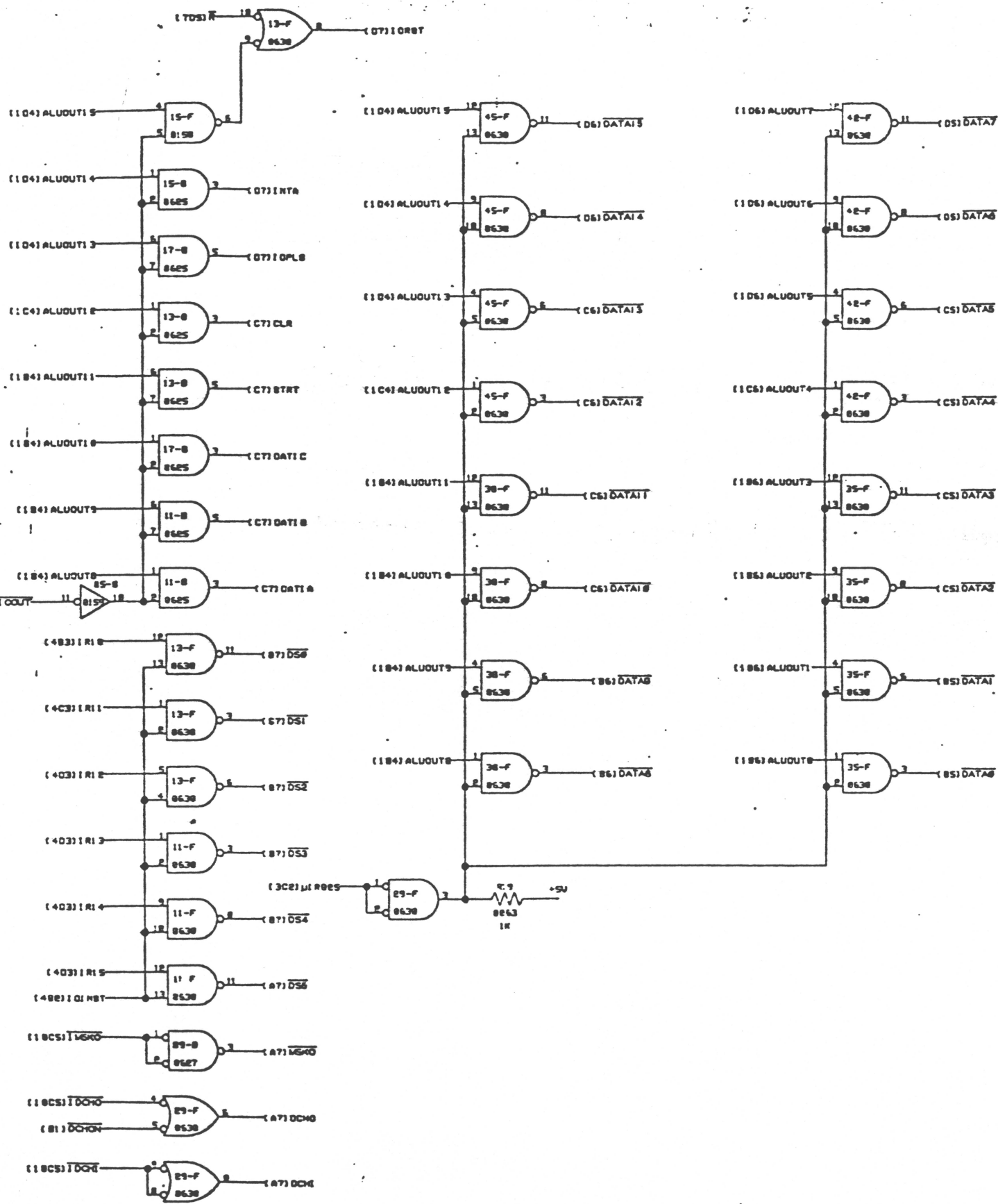


- ERROR TEST POINTS
- TP7 --- (848) NONCAS
  - TP4 --- (A6) TSTART
  - TP3 --- (A6) TWRITE
  - TP1 --- (1845) CLK/DAT
  - TP5 --- (1885) ENBWDR
  - TP2 ---

(TIMING)

DRAWN		DATA GENERAL CORPORATION WESTBORO, MASSACHUSETTS 01581  TITLE  <b>NOVA 4/C</b>  SIZE CODE    DRAWING NUMBER    RE 0    001001600    0
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		

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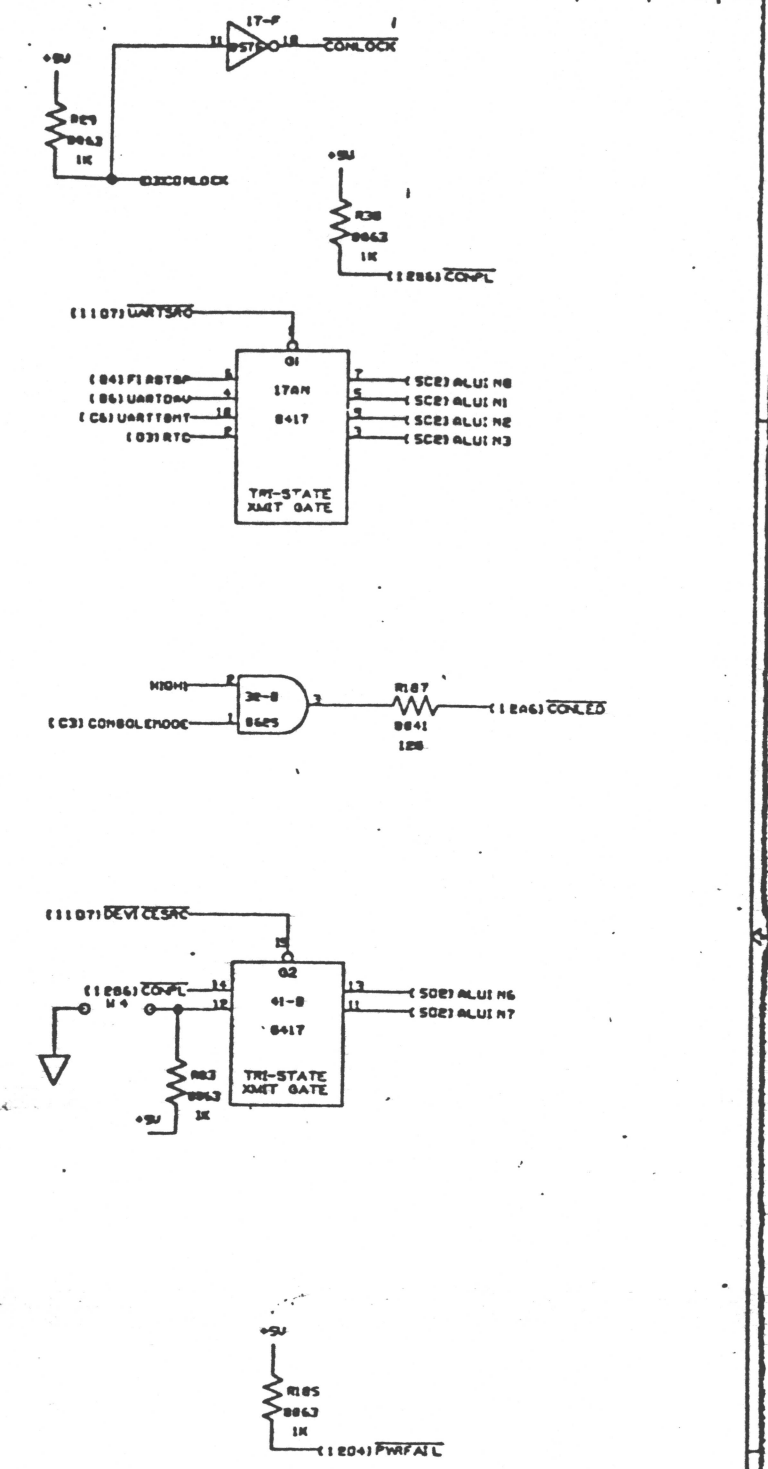
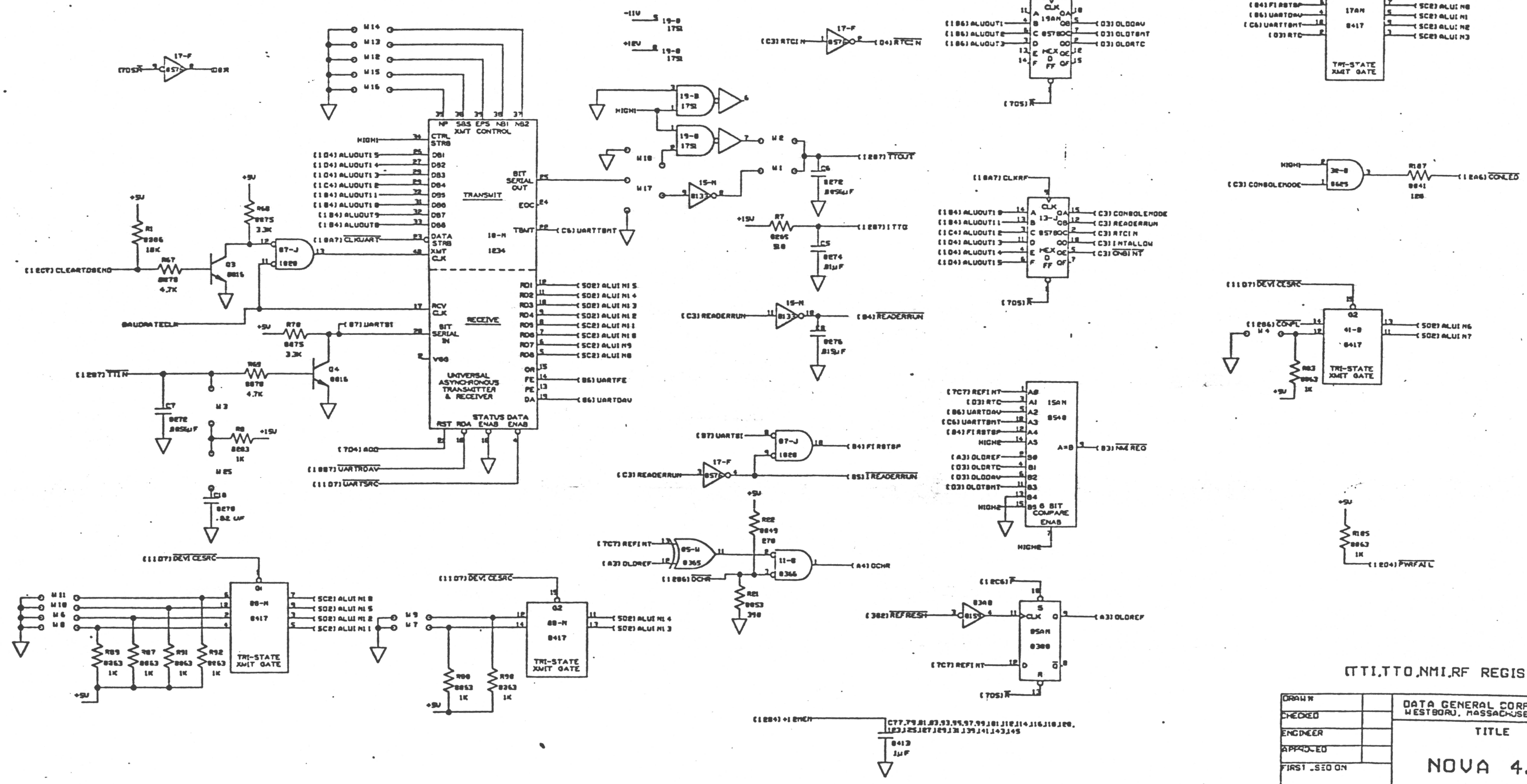
(I/O SIGNALS)

480

DRAWN		DATA GENERAL CORPORATION
CHECKED		WESTBORO, MASSACHUSETTS 01581
ENGINEER		TITLE
APPROVED		NOVA 4/C
FIRST USED ON		SIZE CODE DRAWING NUMBER
		0010016000

THE PURPOSE OF THIS SYMBOL IS TO INDICATE THAT THE PARTS LISTED THEREIN ARE TO BE USED IN THE ASSEMBLY OF THE BOARD OR USED IN THE ASSEMBLY OF THE BOARD FOR MANUFACTURE OR SALE BY THE BOARD OR BY A SUBSIDIARY THEREOF.

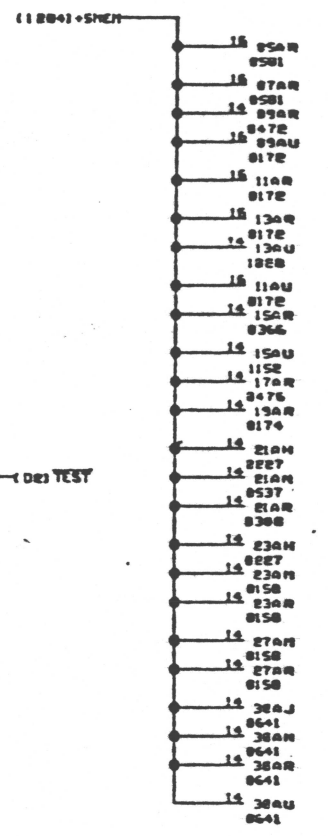
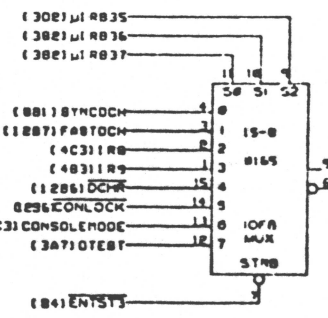
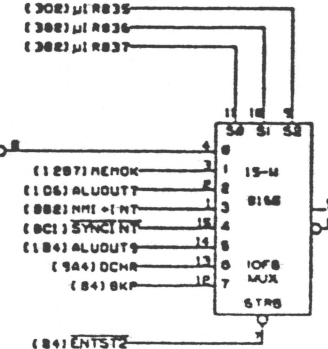
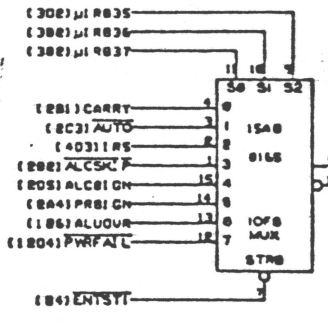
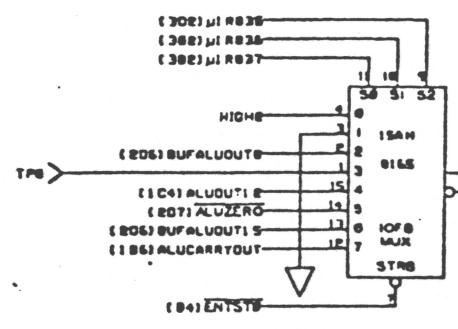
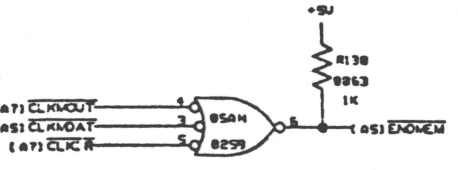
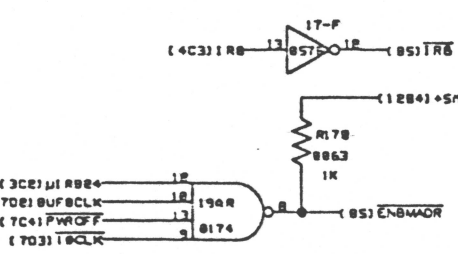
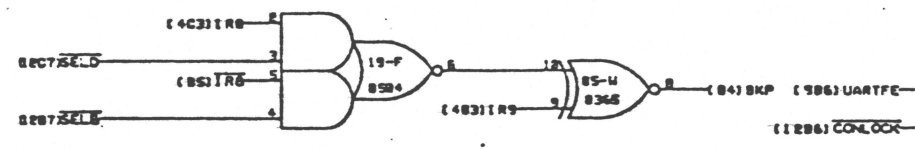
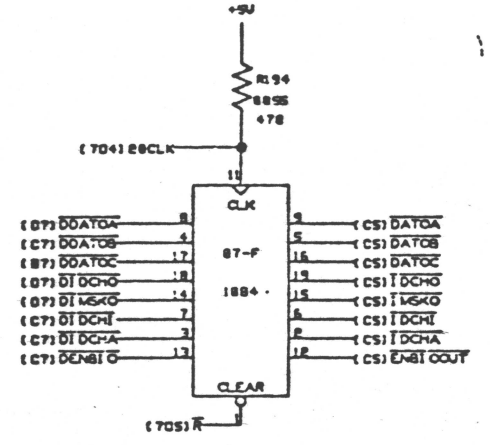
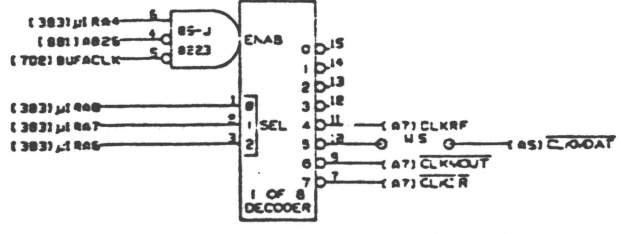
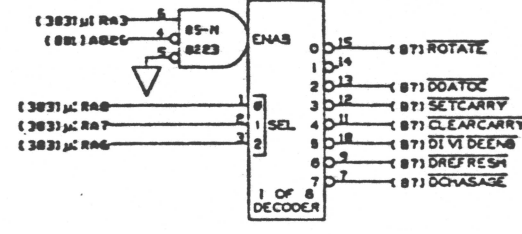
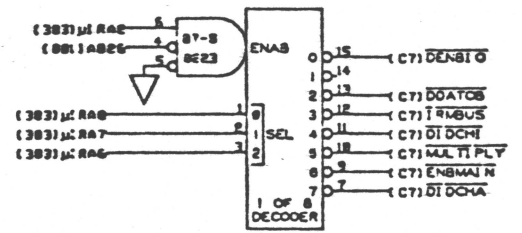
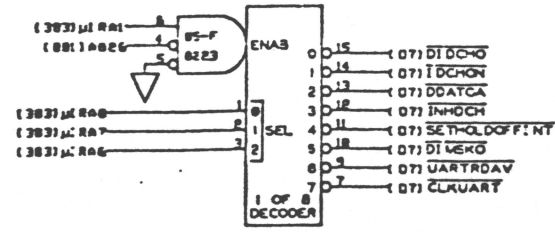
REVISIONS			
REV	DESCRIPTION	DRFTG	APP BY



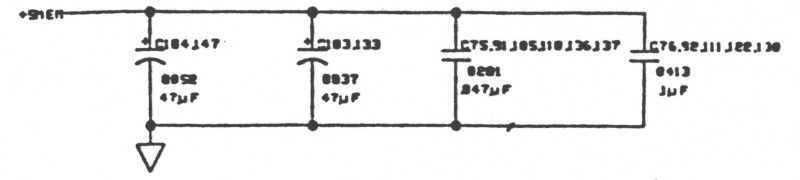
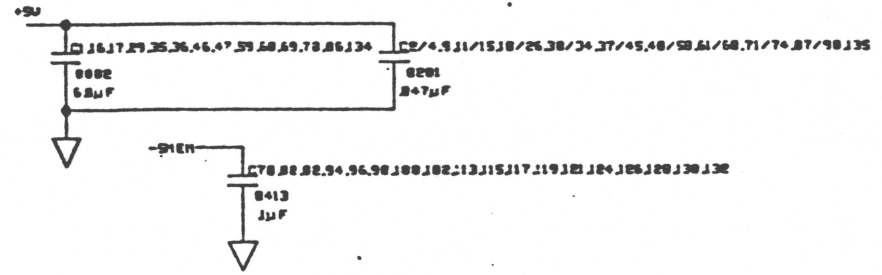
(TTI, TTO, NMI, RF REGISTER)

DRAWN		DATA GENERAL CORPORATION
CHECKED		WESTBORO, MASSACHUSETTS 01581
ENGINEER		TITLE
APPROVED		NOVA 4/C
FIRST SECON		SIZE CODE DRAWING NUMBER
		001001600

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(RANDOM DECODERS. TEST MUX)

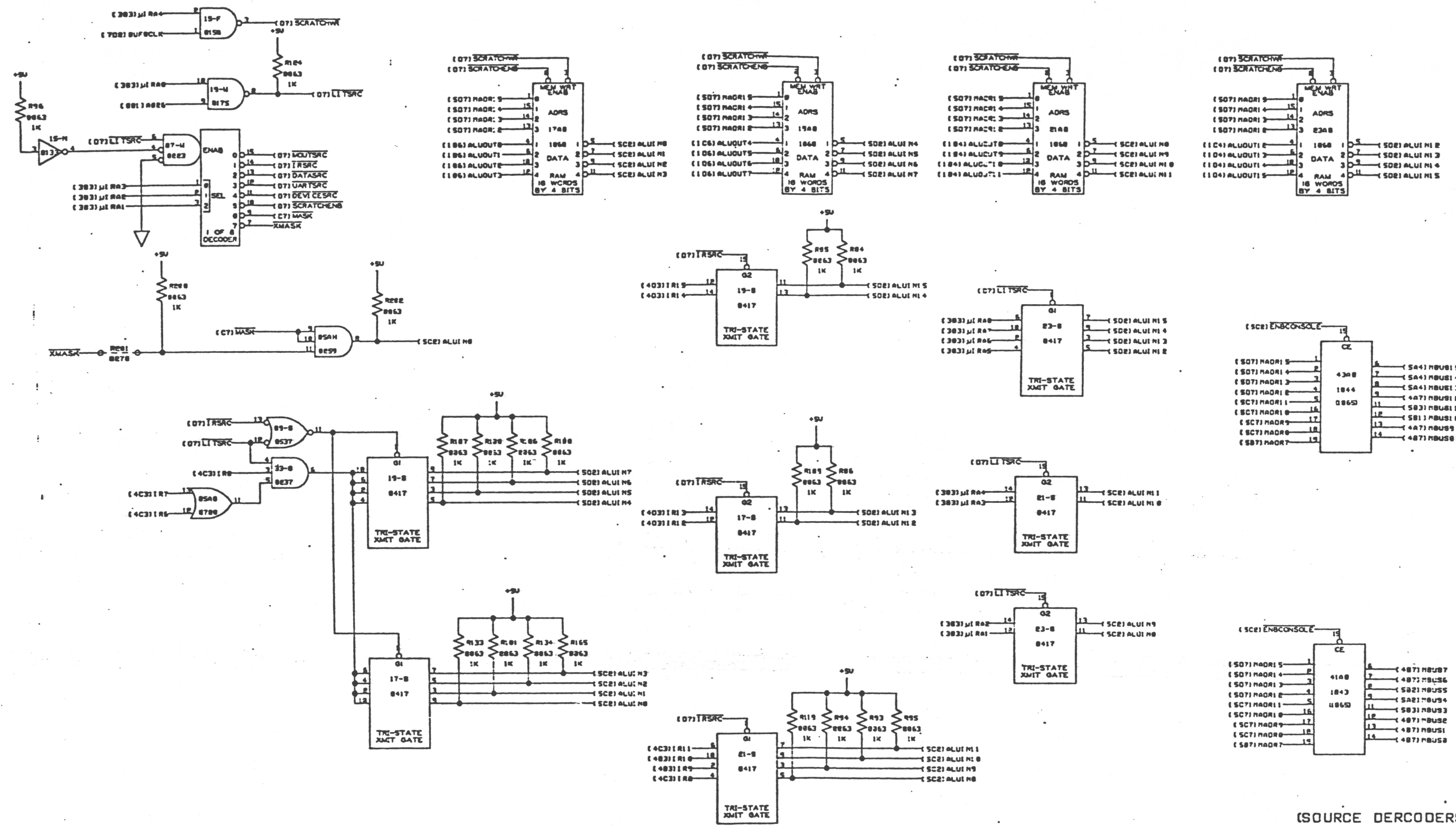
DRAWN		DATA GENERAL CORPORATION WESTBORD, MASSACHUSETTS 01581
CHECKED		
ENGINEER		
APPROVED		
FIRST USED ON		TITLE
		NOVA 4/C
		SIZE CODE
		CRAWING NUMBER
		0010016002
		REV
		10M2

7 6 5 4 3 2 1



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A  
B  
C



(SOURCE DERCODERS, BUFFERS)

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ENGINEER		NOVA 4/C	
APPROVED		SIZE CODE	DRAWING NUMBER
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A001 O (A4)CND. B  
 A002 O (A4)CND. B  
 A003 O (B4)+SU  
 A004 O (B4)+SU  
 A005 O  
 A006 O  
 A007 O  
 A008 O  
 A009 O  
 A010 O (B0)+1SU  
 A011 O  
 A012 O  
 A013 O  
 A014 O  
 A015 O  
 A016 O  
 A017 O  
 A018 O  
 A019 O  
 A020 O  
 A021 O  
 A022 O  
 A023 O  
 A024 O  
 A025 O  
 A026 O  
 A027 O  
 A028 O  
 A029 O  
 A030 O  
 A031 O  
 A032 O  
 A033 O  
 A034 O  
 A035 O  
 A036 O @NEXTADCLK  
 A037 O (B4)MCKO  
 A038 O  
 A039 O (B7)1170  
 A040 O  
 A041 O (B4)CND. B  
 A042 O (B4)CND. B  
 A043 O (B4)CND. B  
 A044 O (B4)CND. B  
 A045 O (B4)CND. B  
 A046 O (B4)CND. B  
 A047 O (B4)CND. B  
 A048 O (B4)CND. B  
 A049 O (B4)CND. B  
 A050 O (B4)CND. B

A051 O (B4)CND. B  
 A052 O (B4)CND. B  
 A053 O (B4)CND. B  
 A054 O (B4)CND. B  
 A055 O (B4)CND. B  
 A056 O (B4)CND. B  
 A057 O (B4)CND. B  
 A058 O (B4)CND. B  
 A059 O (B4)CND. B  
 A060 O (B4)CND. B  
 A061 O (B4)CND. B  
 A062 O (B4)CND. B  
 A063 O (B4)CND. B  
 A064 O (B4)CND. B  
 A065 O (B4)CND. B  
 A066 O (B4)CND. B  
 A067 O (B4)CND. B  
 A068 O (B4)CND. B  
 A069 O (B4)CND. B  
 A070 O (B4)CND. B  
 A071 O (B4)CND. B  
 A072 O (B4)CND. B  
 A073 O (B4)CND. B  
 A074 O (B4)CND. B  
 A075 O (B4)CND. B  
 A076 O (B4)CND. B  
 A077 O (B4)CND. B  
 A078 O (B4)CND. B  
 A079 O (B4)CND. B  
 A080 O (B4)CND. B  
 A081 O (B4)CND. B  
 A082 O (B4)CND. B  
 A083 O (B4)CND. B  
 A084 O (B4)CND. B  
 A085 O (B4)CND. B  
 A086 O (B4)CND. B  
 A087 O (B4)CND. B  
 A088 O (B4)CND. B  
 A089 O (B4)CND. B  
 A090 O (B4)CND. B  
 A091 O (B4)CND. B  
 A092 O (B4)CND. B  
 A093 O (B4)CND. B  
 A094 O (B4)CND. B  
 A095 O (B4)CND. B  
 A096 O (B4)CND. B  
 A097 O (B4)CND. B  
 A098 O (B4)CND. B  
 A099 O (B4)CND. B  
 A100 O (B4)CND. B

B001 O (A4)CND. B  
 B002 O (A4)CND. B  
 B003 O (B4)+SU  
 B004 O (B4)+SU  
 B005 O  
 B006 O  
 B007 O  
 B008 O  
 B009 O  
 B010 O  
 B011 O  
 B012 O  
 B013 O  
 B014 O  
 B015 O  
 B016 O (C6)CND. B  
 B017 O (C6)CND. B  
 B018 O  
 B019 O  
 B020 O  
 B021 O  
 B022 O (C6)TESTRESEY  
 B023 O (C6)F  
 B024 O (C6)F  
 B025 O (C6)F  
 B026 O (C6)F  
 B027 O (C6)F  
 B028 O (C6)F  
 B029 O (C6)F  
 B030 O (C6)F  
 B031 O (C6)F  
 B032 O (C6)F  
 B033 O (B4)DCND  
 B034 O (B4)DCND  
 B035 O (B4)DCND  
 B036 O (B4)DCND  
 B037 O (B4)DCND  
 B038 O (B4)DCND  
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 B043 O (B4)DCND  
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 B046 O (B4)DCND  
 B047 O (B4)DCND  
 B048 O (B4)DCND  
 B049 O (B4)DCND  
 B050 O (B4)DCND

C001 O (B4)CONRSTH  
 C002 O (B4)CONRSTL  
 C003 O (B4)CONRSTL  
 C004 O (B4)CONRSTL  
 C005 O (B4)CONRSTL  
 C006 O (B4)CONRSTL  
 C007 O (B4)CONRSTL  
 C008 O (B4)CONRSTL  
 C009 O (B4)CONRSTL  
 C010 O (B4)CONRSTL  
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 C045 O (B4)CONRSTL  
 C046 O (B4)CONRSTL  
 C047 O (B4)CONRSTL  
 C048 O (B4)CONRSTL  
 C049 O (B4)CONRSTL  
 C050 O (B4)CONRSTL

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7 6 5 4 3 2

DRAWN		DATA GENERAL CORPORATION WESTBORO, MASSACHUSETTS 01581  TITLE  <b>NOVA 4/C</b>  SIZE CODE DRAWING NUMBER 01 001001600
CHECKED		
ENGINEER		
APPROVED		
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