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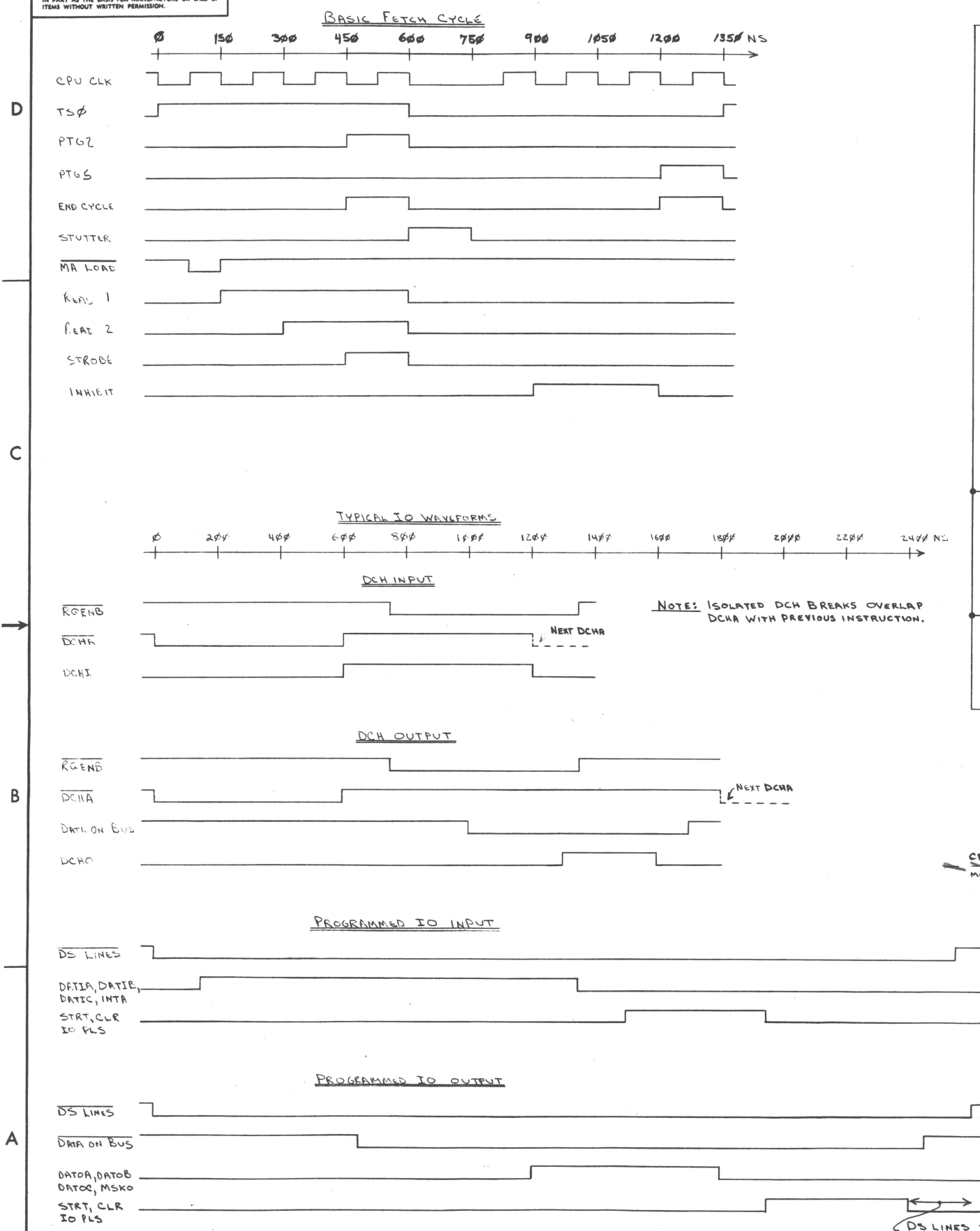
REVISIONS			
REV.	DESCRIPTION	DRFTG.	APP. BY DATE

150 nsec per Nibble

Instr. MBO → MA → MB
MEMBUS to IR, MBO → ADDER, Bits 8 → IR to ADDER → to Prg Cal. into Multiplier then to MBO.

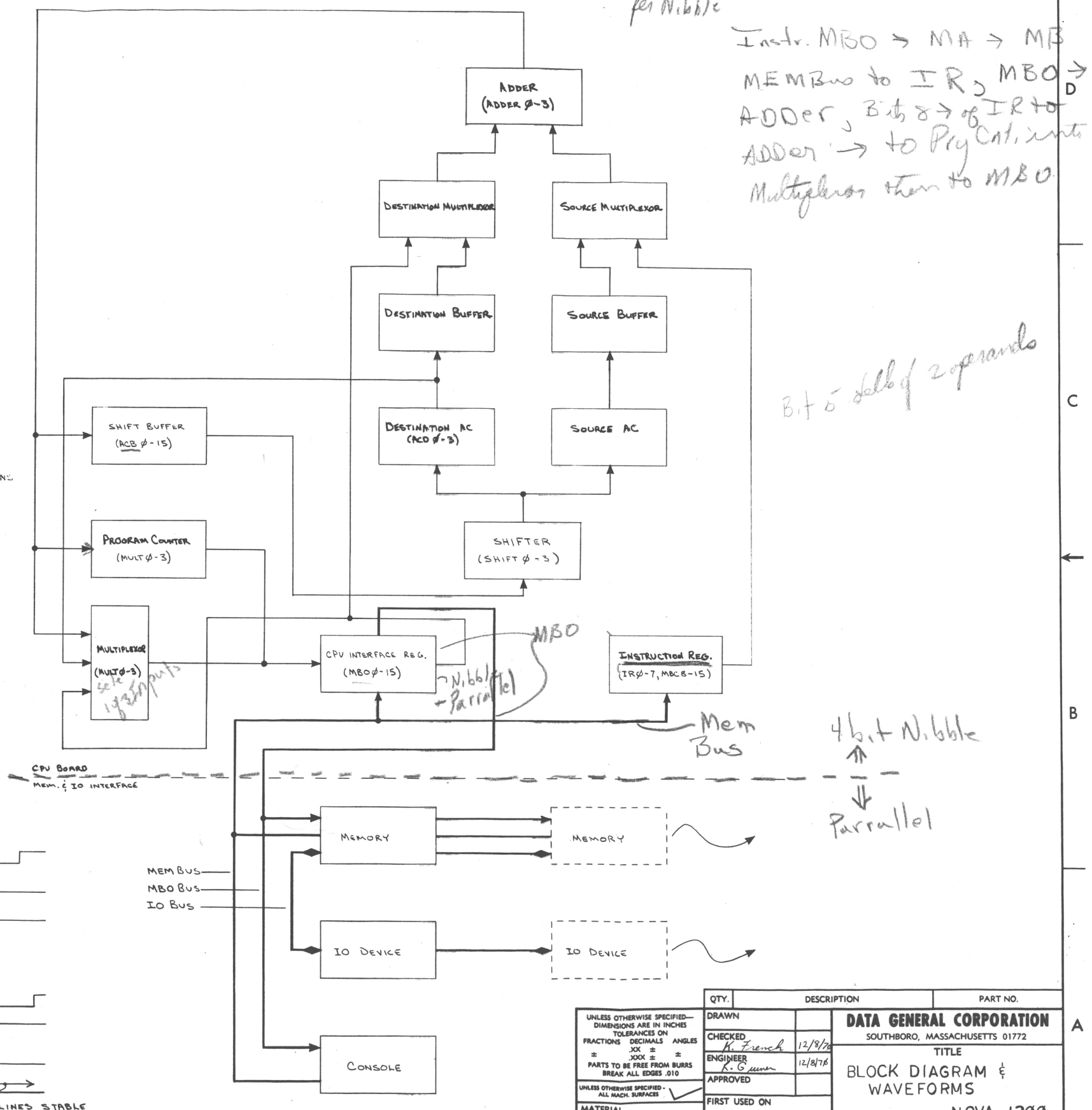
Bit 5 falls of 2 operands

4 bit Nibble
Parallel



NOTE: ISOLATED DCH BREAKS OVERLAP DCHA WITH PREVIOUS INSTRUCTION.

DS LINES STABLE 600 NS AFTER TRAILING EDGE OF STRT, CLR, IO PLS.



QTY.	DESCRIPTION	PART NO.

DRAWN		DATA GENERAL CORPORATION	
CHECKED		SOUTHBORO, MASSACHUSETTS 01772	
ENGINEER		TITLE	
APPROVED		BLOCK DIAGRAM & WAVEFORMS	
FIRST USED ON		NOVA 1200	
MATERIAL	SCALE	SIZE	REV.
		D 001	00
FINISH		DRAWING NUMBER	
		000107	