NOVA SUPER NOVA OPTION

MULTIPROCESSOR COMMUNICATIONS ADAPTER TYPE 4038

Data General's Multiprocessor Communications Adapter, Type, 4038, provides a simple, economical means of connecting several Nova and Supernova computers to form a multiprocessor system. Such a small-computer multiprocessor system is a powerful, highly flexible alternative to a single large computer in many applications.

OPERATION

The Multiprocessor Communications Adapter makes it possible to connect up to fifteen Nova and Supernova computers into a multiprocessor system by permitting blocks of data to be transferred from one computer to another through the computer's data channel facilities. One adapter is attached to the IO bus of each computer, and the adapters are connected via a common communication bus. Each adapter includes an independent receiver and transmitter. A processor with an adapter may establish a logical link between its adapter transmitter and any receiver it designates.

A number of logical links concurrently share the single communications bus, using a time partitioning multiplexer. The multiplexer circuitry is built into the adapter. If there are N logical links established and communications is proceeding on all, each link receives 1/N of the communications bus time. Any of the interconnected computers may be switched off without affecting the computers still in operation.

The bandwidth of the bus is 500KHz (1 million bytes per second). However, this rate will only be obtained when a large number of links are active concurrently. Data rates are primarily determined by the processor's channel facilities. Typical data rates for a single link are 100 KHz for Nova, 140 KHz for Supernova, and 250 KHz for Supernova with high speed data channel option.

Since the receivers and transmitters are data channel devices, each contains a word-count register and an address register, as well as a status register. The word-count register must be initialized to contain the twos complement of the number of words to be transferred, and the address register must be initialized to contain the memory location from which the first word will be taken. The transmitter registers must be initialized by the transmitting processor, and the receiver registers must be initialized by the receiving processor. A transmitter can not force data into a receiving processor at addresses not specified by the receiver.

Each adapter is numbered (1, 2, ... 15), and each contains a 4-bit code in both its receiver status register and its transmitter status register. These codes are used to specify the numbers of the other adapters to which the adapter is to be connected. When the number of a transmitter is set into the receiver by the transmission of a data word to that receiver, the receiver will accept further data only from that transmitter, i.e., it "locks" to that transmitter. An IO instruction is required to "unlock" the receiver so that it can receive data from another transmitter.

The size and nature of the data transmission can be established by convention. In a relatively simple system in which the size and nature of the data blocks to be transferred is known in advance, the receiver can initialize itself to accept the next block at the completion of the previous transmission.

If the exact size and nature of the data blocks is determined dynamically, a control block specifying the

nature of a transfer must be transmitted before a data block can be transmitted. The receiver initializes itself to accept a control block of standard format and unlocks itself. The first word transferred to the receiver locks it to the sending transmitter by setting the transmitter until explicitly unlocked by the program. Thus, once the control block is received, the receiver can be initialized to accept the data from the appropriate transmitter. Alternatively, if the control block from adapter A to adapter B is a request for data, then adapter B's transmitter can be started sending data while its receiver is re-initialized to accept a new control block. The hardware does not explicitly distinguish between data and control blocks.

APPLICATIONS

In situations characterized by relatively simple mathematical operations and substantial data communications and formatting requirements, a small computer multiprocessor system is less expensive and far more flexible than any single medium-to large-scale computer capable of meeting all the job requirements. Because several compatible processors are used, the system provides its own backup in case of failure. In many cases a multiprocessor system can also provide emergency backup for a large-scale computer in the same system, eliminating the need for a second large computer.

In a typical multiprocessor system, one small computer might handle a number of data communication lines while another computer pre-processes data, and a third performs the actual computations.

In conjunction with a large-scale central processor, a multiprocessor system might handle all data communications and formatting functions, as well as computations at a specified level of complexity, while very large or highly complex computations are handled by the central processor.

In this sort of hierarchical data processing system, computers of varying size and capability are matched to a variety of functions. This hierarchical approach makes it possible to construct computer systems which match precisely the requirements of a situation and which are able to respond dynamically to changing situations.

IO INSTRUCTIONS

The multiprocessor communications adapter (MCA) contains independent receiver (MCAR) and transmitter (MCAT) subsections. Each has its own status register for control as well as independent word count, address, and data registers.

For the receiver, BUSY and DONE are controlled or sensed by bits 8 and 9 in all IO instructions with device code 7, mnemonic MCAR. For the transmitter, BUSY and DONE are controlled or sensed by bits 8 and 9 in all IO instructions with device code 6, mnemonic MCAT. Interrupt disable is controlled by interrupt priority mask bit 12 for both.

Receiver

The MCA receiver sets DONE, clears BUSY, and interrupts the processor if:

a) the last word in a receiver's specified block is received (bit 15 of the receiver status register is set), or

b) the last word in a transmitter's specified block is received (bit 14 of the status register set) even if a longer block was specified by the receiver, or

c) the receiver timed out (bit 12 set).

The Clear function clears BUSY and DONE as well as bits 12 through 15 of the receiver status register, the receiver is disabled and unlocked. The Start function clears DONE, clears bits 12, 14, and 15, and sets BUSY, enabling the receiver to accept data from a transmitter.

DIA - MCAT

DOA - MCAR

Read/load the receiver current address (CA) register from the selected accumulator. The register specifies the address of the next word to be stored into the processor's memory.

DIB - MCAR

DOB - MCAR

Read/load the receiver word count (WC) register from the selected accumulator with the twos complement of the number of words to be received. If read at the end of a transfer, the register contains the twos complement of the number of words yet to be received.

DIC - MCAR

Read the receiver status register according to the format below. These bits are set in the adapter when DONE is set.

- 0-3 Code of the receiver (1-15) as set by its jumpers.
- 4-7 When Locked, the code of the transmitter to which the receiver is logically connected (1-15). The transfer of a single word to a receiver sets these bits in the receiver status register to the code of the sending transmitter and makes the receiver go locked, insuring that it will accept no data from any other transmitter.
- 8-11 - Unused
- 12 - Timeout: data transmission has been in progress, but no new data has been sent in the last 10 milliseconds. This usually means that power is off in the transmitter's processor. This timeout does not occur if the transmitter word count goes to zero, indicating a shorter block length than the receiver's.
- 13 - Locked: the receiver has begun accepting data from a transmitter.
- 14 - Transmitter has sent the last word of a block as specified by its WC.
- 15 - Receiver WC went to zero indicating that the transfer specified by the receiver has been completed.

Transmitter

The MCA transmitter sets DONE, clears BUSY, and interrupts the processor if:

a) the last word in a receiver specified block is sent (bit 15 of the transmitter's status register is set,
b) the last word in a transmitter specified block is sent (bit 14), or
c) the transmitter timed out (bit 12).

The Clear function clears the BUSY and DONE in the transmitter's status word. Since BUSY is cleared, transmission is stopped. If transmission were in progress when the instruction was issued, a word might be lost. The Start function clears DONE and sets BUSY, initiating the block transfer specified by the transmitter CA, WC and status registers.

DIA - MCAT
DOA - MCAT
Read/load the transmitter current address (CA) register from the selected accumulator. The register specifies the address of the next word to be stored into the processor's memory.
DIB - MCAT
DOB - MCAT
Read/load the transmitter word count (WC) register from the selected accumulator with the twos complement of the number of words to be transmitted. If read at the end of a transfer, the register contains the twos complement to be transmitted.
DIC - MCAT
DOC - MCAT
Read/load the transmitter status register according to the following format. Note that only bits 0-3 may be changed with a DOC instruction and that bits 12-15 are valid only when done is set.

0-3 - Code of the receiver desired (1-15).
4-7 - Code of the transmitter as set by its jumpers.
8-11 - Unused
12 - Timeout: data transmission has been attempted but the selected receiver has not acknowledged within the last 10 milliseconds. This means either that power is off in the selected receiver's processor or that it is locked to another transmitter. The timeout does not occur if the receiver word count goes to zero indicating a shorter word length than the transmitter's.
13 - Locked: the designated receiver is locked to some transmitter.
14 - The transmitter word count went to zero indicating that the block transmission has been completed.
15 - The receiver word count went to zero.

INSTALLATION

The Multiprocessor Communications Adapter is mounted on a 15-inch square printed circuit board and plugs directly into one of the seven standard subassembly slots in the Nova or Supernova chassis.

Each adapter contains four jumpers that are set by the user to assign a code to the receiver/transmitter pair. The code is set to 15 when the adapter is shipped.

The data rate of the bus also can be adjusted by the user. The 500KHz rate is supplied as standard, but it may be reduced to 300KHz in order to lengthen the maximum bus length to 150 feet from the standard 75 feet.

Each adapter contains a terminator network for the communication bus. In a system containing two adapters, the terminator networks operate as supplied. In systems containing more than two adapters, the terminators must be removed from all adapters except those at the ends of the communications bus. To do this, the user removes all 220 ohm and 270 ohm resistors from the middle adapters.

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