DataGeneral

Customer Documentation

Technical Notice for AViiON™ 3000 and 4000 Series Systems: Programming System Control and I/O Registers

AViiON™
PRODUCT LINE

Technical Notice for AViiON™ 3000 and 4000 Series Systems: Programming System Control and I/O Registers

014-001878-00

Ordering No. 014-001878

Printed in the United States of America
Rev. 00, June 1990

Notice

Technical Notice for
AViiON™ 3000 and 4000 Series Systems:
Programming System Control and I/O Registers
014-001878-00
014-001879-00 (Japanese version)

Revision History:

Original Release - June 1990

A vertical bar in the margin of a page indicates substantive technical change from the previous revision.

How to Use this Technical Notice

Use this technical notice in conjunction with the programming manual *AViiON™ 300 and 400 Series Stations: Programming System Control and I/O Registers* (014-001800) to program 3000 and 4000 series systems. These pages identify how a 3000 or 4000 series system differs from 300 and 400 series stations. Insert these pages into the programming manual as described in the section "Updating Instructions" that follows.

This technical notice affects the programming manual as follows:

Chapter 1	System Board Architecture See changes enclosed.
Chapter 2	Programming the System Board Items or sections labeled 400 series only do apply to 3000 and 4000 series systems. Disregard items or sections labeled 300 series only, they do not apply to 3000 and 4000 series. All addresses are the same as addresses for 400 series systems.
Chapter 3	Interrupts, System Errors and Bus Faults Items or sections labeled 400 series only do apply to 3000 and 4000 series systems. Disregard items or sections labeled 300 series only, they do not apply to 3000 and 4000 series. All addresses are the same as addresses for 400 series systems.
Chapter 4	Programming the Monochrome Graphics Subsystem Because the 3000 and 4000 series stations do not support graphics, disregard this chapter.
Chapter 5	Programming the Color Graphics Subsystem Because the 3000 and 4000 series stations do not support graphics, disregard this chapter.
Chapter 6	Programming the Keyboard Interface and Speaker Because the 3000 and 4000 series stations do not support a keyboard, disregard this chapter.
Chapter 7	Programming the Serial Ports and Parallel Port See changes enclosed.
Chapter 8	Programming the Local Area Network No changes.
Chapter 9	Programming the Small Computer System Interface No changes.
Appendix A	Address Map No changes.
Appendix B	Power-up Flowchart No changes.
Appendix C	Boot File Format No changes.
Appendix D	System Board Connectors See changes enclosed.

Updating Instructions

To update your copy of *AViiON™ 300 and 400 Series Stations: Programming System Control and I/O Registers*, please remove the pages from the manual and insert the technical notice pages into the manual as follows:

Remove	**Insert**
Contents	Contents
Tables	Tables
Figures	Figures
1-1 through 1-4	1-1 through 1-4
1-9/1-10	1-9/1-10
2-7/2-8	2-7/2-8
2-15/2-16	2-15/2-16
3-1/3-2	3-1/3-2
3-11 through 3-16	3-11 through 3-16
7-1 through 7-2	7-1 through 7-2
D-1 through D-6	D-1 through D-6
D-11/D-12	D-11/D-12

Insert the Cover page immediately after the Cover page of the manual.

Insert the Title/Notice page immediately after the Title/Notice page of the manual.

Insert "How to Use this Technical Notice" immediately after the Preface of the manual.

Contents

Chapter 1 – System Board Architecture

Chapter 2 – Programming the System Board

Chapter 3 - Interrupts, System Errors, and Bus Faults

Chapter 4 - Programming the Monochrome Graphics Subsystem

Chapter 5 – Programming the Color Graphics Subsystem

Chapter 6 – Programming the Keyboard Interface and Speaker

Chapter 7 - Programming the Serial Ports and Parallel Port

Chapter 8 - Programming the Local Area Network Interface

Chapter 9 – Programming the Small Computer System Interface Port

Appendix A – Address Map

Appendix B – Power–Up Flowchart

Appendix C – Boot File Format

Appendix D – System Board Connectors

Index

Documentation Set

Tables

Table

Figures

Figure

Chapter 1
System Board Architecture

This chapter describes the system board architecture, including the following topics:

- System architecture and configuration.
- System board architecture and configuration.
- The CPU set, including the CPU and CMMUs and cache coherency.
- Main memory and the memory interface.
- The Mbus and Sbus, and the interface between them.
- The graphics subsystem, including monochrome graphics, color graphics and the Z-buffer controller (400 series only).
- The I/O subsystem, including the keyboard port, serial ports, parallel port, Ethernet LAN interface, SCSI interface, and VMEbus interface (400 series only). The VMEbus section discusses VMEbus arbitration and VMEbus data transfers.
- Timers available to system programmers.
- Interrupts and the interrupt control logic.

Architecture and Configuration

Data General's AViiON™ 3000 and 4000 series systems use the Motorola 32-bit MC88100 RISC (Reduced Instruction Set Computing) processor and the Motorola MC88200 CMMU (Cache/Memory Management Unit). They run either Data General's DG/UX™ operating system or industry-available operating systems for MC88000-based systems. Figure 1-1 and Figure 1-2 illustrate the system board architecture.

Using 4-Mbyte memory modules, 3000 series systems support 16 Mbytes maximum and 4000 series systems support 32 Mbytes maximum.

Both 3000 and 4000 series systems have internal disk and tape storage which is made possible through a SCSI interface. In addition for 4000 series systems, a compact, free-standing, mass-storage subsystem is available for additional disk or tape storage.

3000 and 4000 series systems do not support graphics.

Table 1-1 summarizes the configurations for 3000 and 4000 series systems.

Table 1-1 System Configurations

Item	3000 Series	4000 Series
CPU set (1 CPU, 2 CMMUs)	1	1 or 2
CPU clock speed (Mhz)	16.67	16.67 or 20
DRAM (4-Mbyte modules)	4 - 16 Mbytes	4 - 32 Mbytes
VMEbus interface	1 slot	2 slots
Integrated I/O		
Parallel port (Centronics or Data Products)	1	1
Serial ports (RS-232-C)	2	2
SCSI ports	1	1
SCSI connectors - internal	4	4
SCSI connectors - external	0	1
LAN interface	1	1

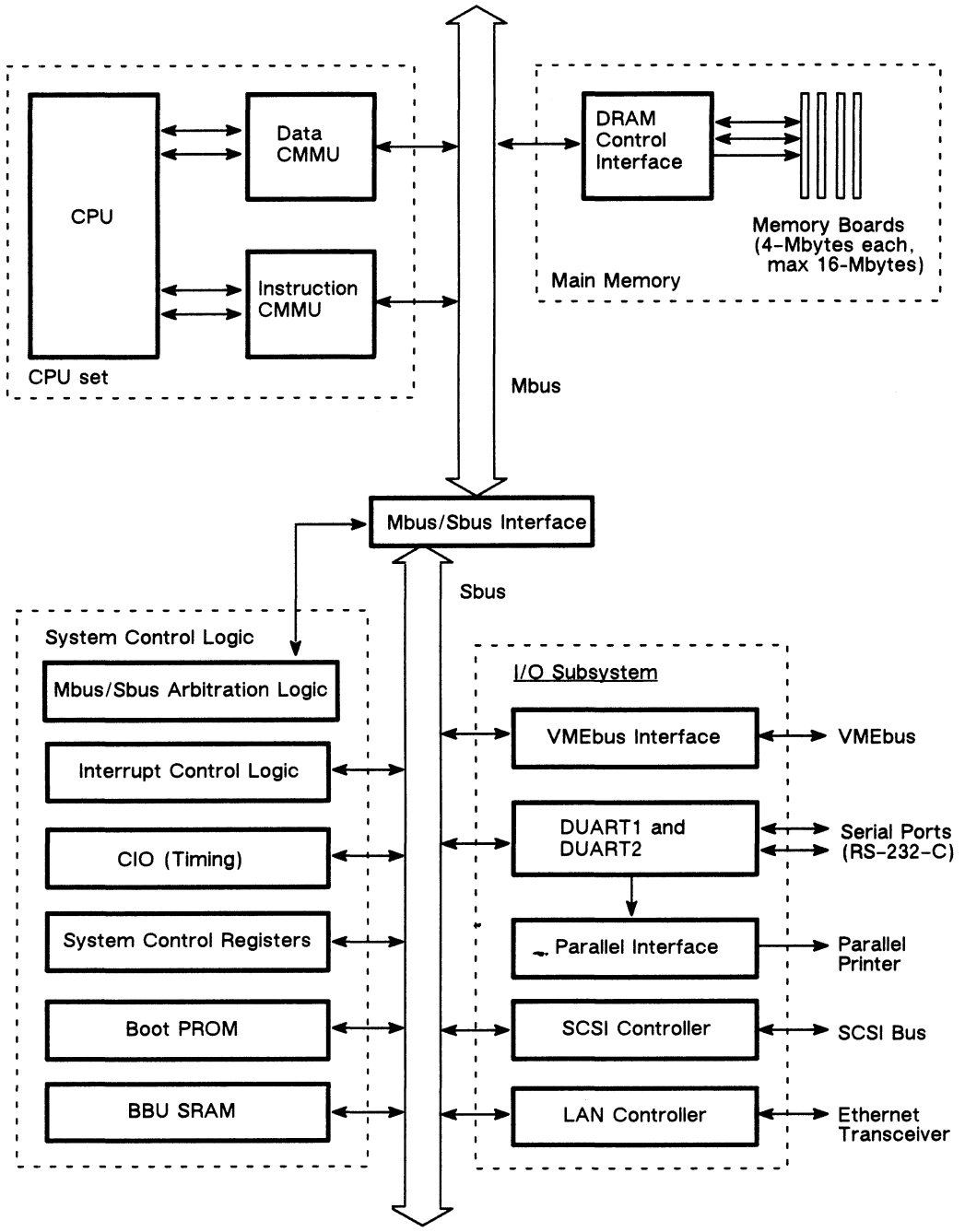


Figure 1–1 System Board Architecture – 3000 Series Systems

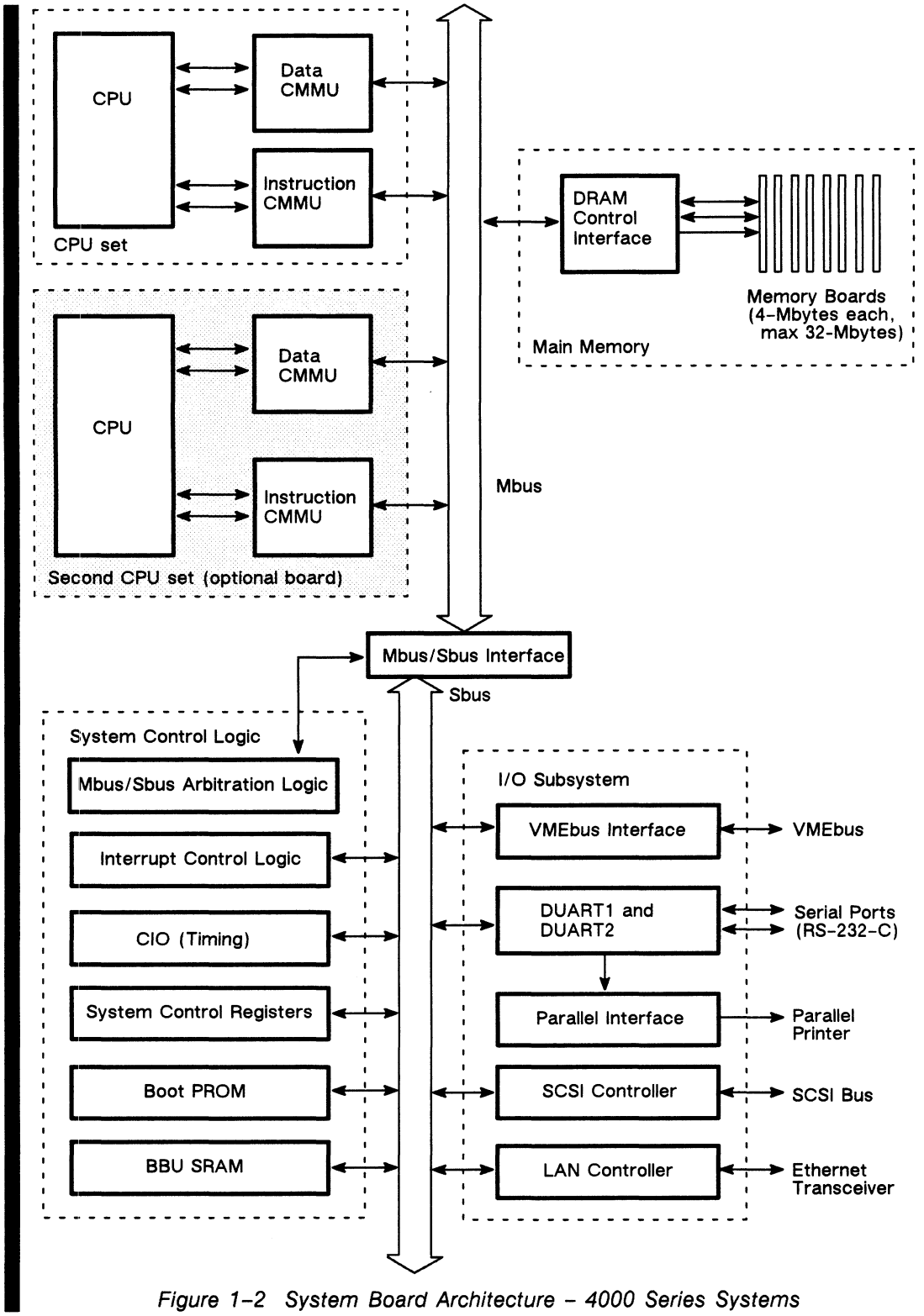


Figure 1–2 System Board Architecture – 4000 Series Systems

Memory

The memory system consists of main memory, which includes onboard dynamic random-access-memory (DRAM), expansion DRAM boards and the associated memory interface logic, plus static RAM (SRAM) and programmable read-only-memory (PROM).

Main Memory

Main memory consists of dynamic random-access-memory (DRAM) and the memory interface logic needed to control accesses to the DRAM (see NO TAG). DRAM memory consists of 4-Mbyte memory modules that plug into the system board. Each 4-Mbyte memory module has 36 1-Mbit, fast-page 100-ns DRAMs that provide 32 data bits and 4 parity bits for each address.

3000 series systems accept as many as four memory modules, for a maximum of 16 Mbytes of RAM. The memory modules plug into the system board.

4000 series systems accept as many as eight memory modules, for a maximum of 32 Mbytes of RAM. The memory modules plug into the system board.

Main memory is contiguous and begins at address 0000 0000. Each location has 36 bits: 32 bits for the data word and 4 bits for parity. The parity logic, located on the system board, generates and checks the parity bits.

The DRAM uses byte parity; one parity bit for each byte of data. The parity bits have separate data-in and data-out connections to the DRAMs, and the write parity data is driven to the DRAMs in a way that allows diagnostic software to force parity bits high during a write to memory. This logic also provides the control signals for refreshing the DRAM array.

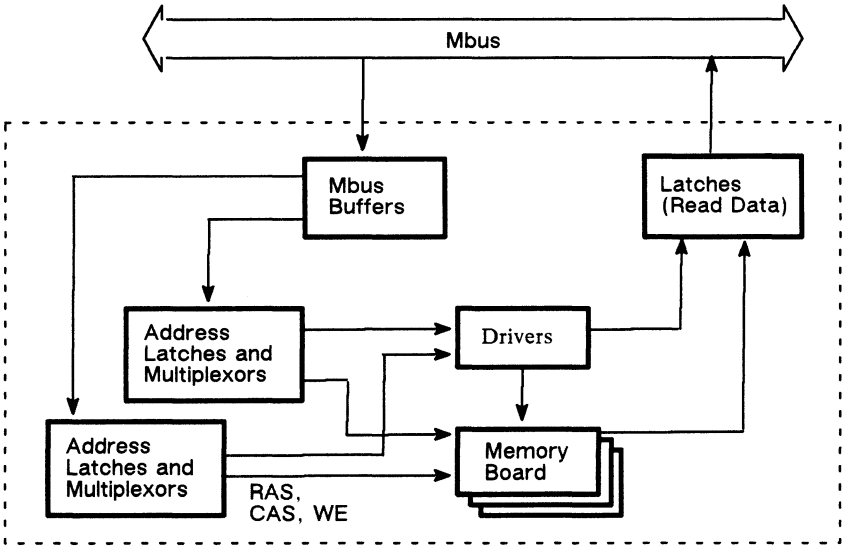


Figure 1-6 Main Memory

Main-Memory Interface

The memory interface connects the DRAM to the Mbus, controlling data transfers to and from the DRAM. When a device addresses memory, the memory interface enables the memory module that contains the addressed location; then reads from or writes to the location. The interface consists of the following:

- Address and data latches.
- Address and data drivers.
- Control logic and memory timing to regulate the memory strobes (RAS and CAS) and write enable (WE).

The memory interface responds only to addresses in the lower 128 Mbytes of system address space. Table 1–3 shows the number of clock cycles it takes to execute reads and writes.

Table 1–3 Memory Read and Write Cycles

Type of Access	Number of Clock Cycles at CPU Speed: 16.67 (MHz)	20 (MHz)
Single-word write	5	6
Single-word read	6	7
Block write (4 words)	11	12
Block read (4 words)	12	13

The memory interface sends status signals to the workstation's Parity Address Register (PAR) to indicate when one or more modules has 100 ns DRAMs installed and the number of modules with 4–Mbit DRAMs. For information on these status bits, see the description of the Parity Address Register (PAR) later in this chapter.

Battery Backed Up (BBU) SRAM and PROM

The BBU SRAM provides 2 Kbytes of nonvolatile storage for diagnostics, system configuration, and boot information. (Note that within this manual we also refer to the BBU SRAM as NOVRAM or nonvolatile RAM.) The 128–Kbyte PROM contains powerup diagnostic and initialization code, including the local code for booting the system over an Ethernet. The diagnostic registers provide information that allow diagnostic software to control the state of the system board, determine system board status, and obtain Mbus parity error status information.

Addressing System Board Resources and System Memory

This section describes how to address the system board resources and system memory. The following numbered steps, in conjunction with Figure 2–2 and Figure 2–3, describe how the CPUs access the system board resources and the system memory.

1. The CPU puts a 32-bit address onto the Mbus.
2. The address decode logic decodes the address bits (2a) and enables access to a device (2b) such as onboard memory, expansion memory boards, utility space, and VME space.
3. The 32-bit address points to a location within the selected device.

Figure 2–2 shows how the CPU addresses memory, while Figure 2–3 shows how addresses are decoded.

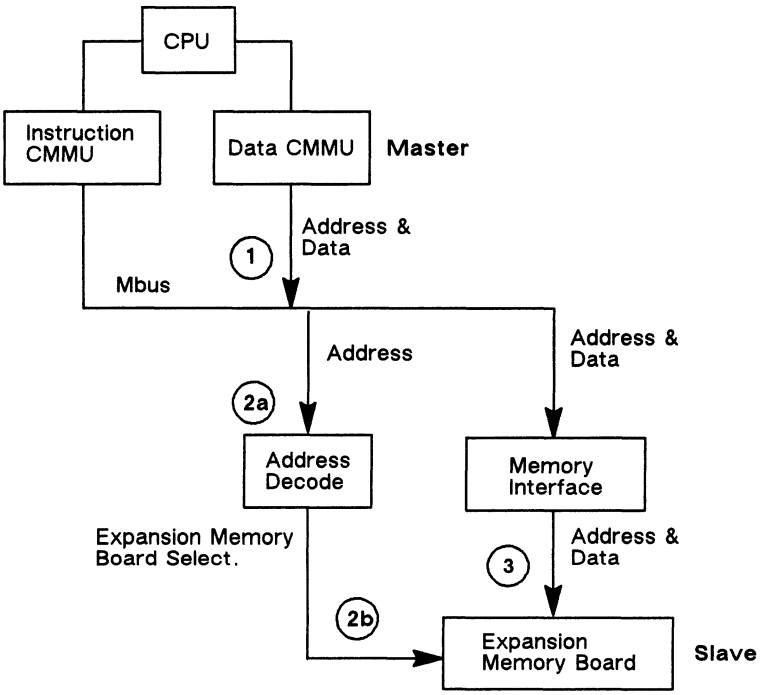


Figure 2–2 How the CPU Addresses System Memory

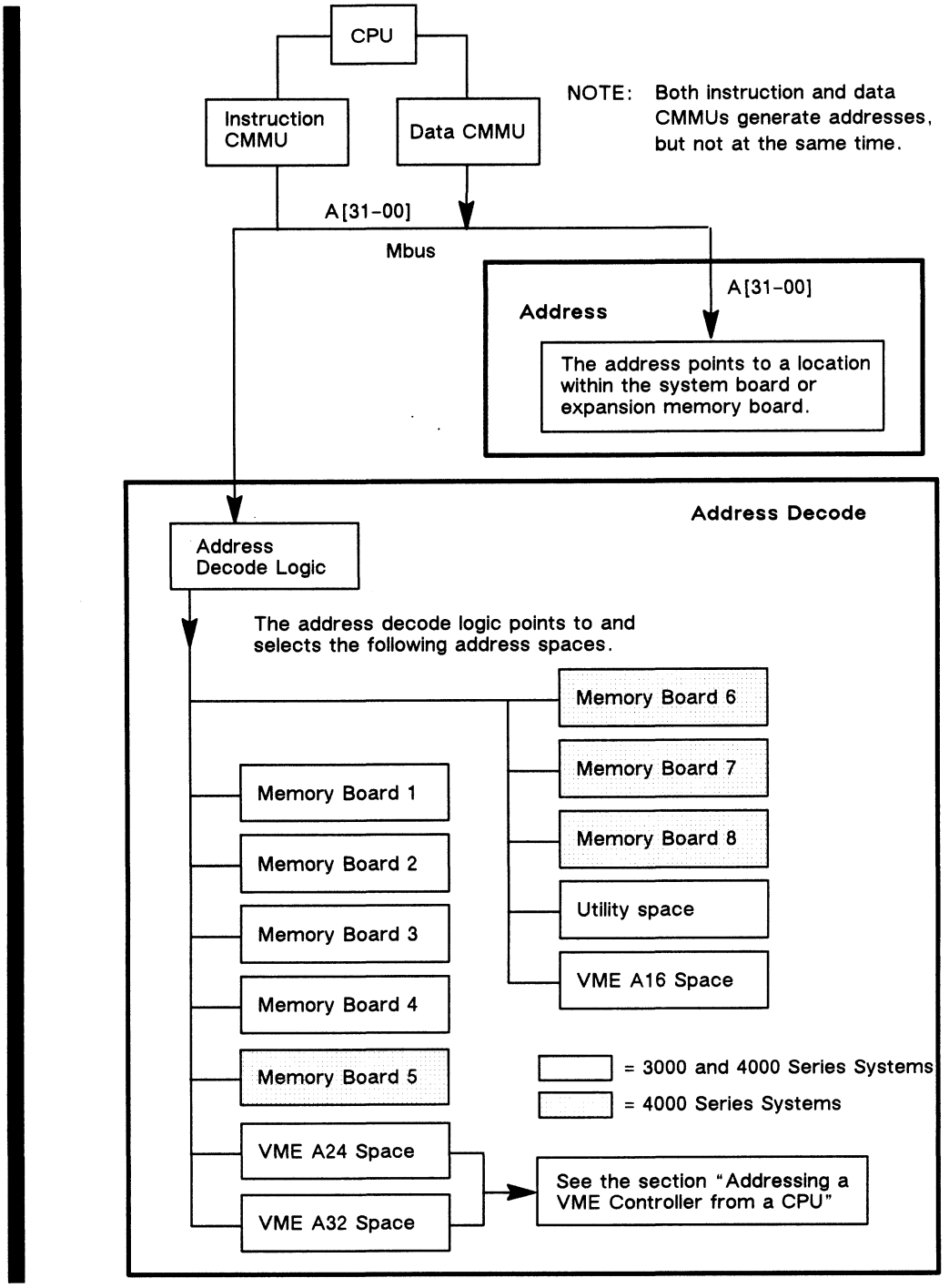


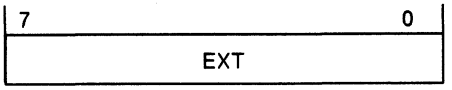
Figure 2-3 Decoding Addresses from the CPU

EXTAD — Extended Address

Address FFF8 8010 — Write only

The extended address register provides the upper eight Mbus address bits when an A24 VMEbus device accesses the Mbus. EXTAD is loaded during powerup with a base address for VME access to system memory.

EXTAD is not affected by either system reset or local reset.



Bit	Mnemonic	Function
7-0	EXT[31-24]	Extended Address. Supplies the address bits A[31-24] to the Mbus when an A24 VMEbus device accesses the Mbus.

Programming the System Control Registers

The system control registers are memory-mapped and are accessed as 32-bit registers. To access a system control register declare it as type **int** in a C program, or use the Load Register from Memory (**ld**) or Store Register to Memory (**st**) instruction in an assembly language program. Table 2-5 identifies the system control registers and their addresses. The rest of this section describes the diagnostic registers.

Table 2-5 Memory Map of the System Control Registers

Register or Component	Address (hexadecimal)	Type
DCR (Diagnostic Control)	FFF8 40C0	Write-only
DSR (Diagnostic Status)	FFF8 40C4	Read-only
PAR (Parity Address)	FFF8 40C8	Read-only
WHOAMI (CPU Configuration)	FFF8 8018	Read-only

Chapter 3
Interrupts, System Errors, and Bus Faults

This chapter discusses the following topics:

- Types of interrupts.
- How the interrupting devices interrupt the CPU.
- How the CPU handles the interrupts.

The workstation has two error reporting mechanisms: bus faults and interrupts. The CMMUs inform the CPU of bus faults, and the interrupt control logic informs the CPU of interrupts generated by the various subsystems.

Interrupts are a means for various system resources (memory, I/O controllers, power supply, etc.) to notify the CPU of a condition that needs attention. Each interrupt has an associated interrupt service routine that the CPU executes. Some interrupts represent a specific interrupt condition (condition-specific interrupts), while others represent one of many possible interrupt conditions (multiple-use interrupts). For specific interrupts, the operating system developer may use a table to associate an interrupt vector with the interrupt. For the multiple-use interrupts, the interrupting device must supply an interrupt vector to the system board CPU.

Interrupt control logic provides the CPU with interrupt information. When devices assert their interrupt request, the interrupt control logic first performs a logical AND of the interrupt requests with the contents of the interrupt mask register; then it asserts the interrupt line (INT) to the CPU. Workstations with two CPUs have two interrupt lines (INT0 and INT1), one for each CPU. In these systems, the interrupt control logic asserts the appropriate line or lines, depending on the masks.

The interrupt service routine reads the interrupt status register (ISR or IST) and if necessary the interrupt enable registers (IENn); then it isolates the interrupt(s).

The device faults for the I/O subsystems are discussed in the related chapters as follows:

Chapter 6 "Programming the Keyboard Interface and Speaker"

Chapter 7 "Programming the Serial Ports and Parallel Port"

Chapter 8 "Programming the Local Area Network Interface"

Chapter 9 "Programming the Small Computer System Interface"

Types of Interrupts

Interrupts fall into one of two categories: condition-specific interrupts and multiple-use interrupts.

Condition-Specific Interrupts

Condition-specific interrupts span much of the system, including all of the local system board interrupts and many VME interrupts. These interrupts represent specific conditions such as the depressing of the abort switch or the occurrence of a single-bit memory read error.

3000 and 4000 Series Interrupts

The condition-specific interrupts include Abort Pushbutton (ABT), AC Failure (ACF), Bus Arbitration Timeout (ATO), Parity Error (PAR), CIO Interrupt (CIO), System Failure (SF), Parallel Port Interrupt (PPI), DUART1 Interrupt (DT1), DUART2 Interrupt (DT2), Ethernet Controller Interrupt (ECI), DMA Terminal Count (DTC), DMA Write Protect Error (DWP), DMA Valid Bit (DVB), and SCSI Controller Interrupt (SCI). Of these, the DUART Interrupts (DI1 and DI2) and the CIO Interrupt (CIO) may be one of several possible, but specifically defined, interrupts from the related device.

Multiple-Use Interrupts (3000 and 4000 Series)

Multiple-use interrupts include Signal High Priority (SHP), Signal Low Priority (SLP), Software-Generated Interrupts (SI[7-0]), and VME Interrupts (IR[7-1]). VME interrupts are generated by VME controllers through seven interrupt request lines (IRQ[7-1]*) on the VMEbus. A VME controller can choose which interrupt line to use when it has an interrupt condition that requires servicing by the system board. These interrupt lines are not limited to specific interrupts; any serviceable interrupt can be generated through the VME interrupt request lines. To execute the correct interrupt service routine, the system board CPU must obtain the interrupt vector from the interrupting VME controller.

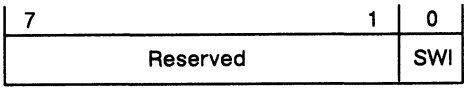
Besides being interrupted, the system board CPU can initiate interrupts to the VME controllers using the VME-level interrupts. The CPU, when it interrupts a VME controller, must define the interrupt level and provide the VME controller with an interrupt vector. This process is described later in this chapter in the section "Interrupting a VME Controller."

SWIR (300 Series Only) — Software Interrupt

Address FFF8 4014 — Write Only

The Software Interrupt Register (SWIR) initiates software interrupts.

The SWIR bits are defined as follows:



Bit	Name	Function
7–1	Reserved	Ignore these bits.
0	SWI	Software interrupt. 1 Interrupts the CPU. The status of this bit is reflected by ISR bit 9 (SI). Writing a 0 to IER bit 9 masks this interrupt. 0 Clears the interrupt request. This bit is not set to 0 after system reset or power-on reset.

Even though a reset does not enable the software interrupt request, software must ensure that bit 0 of the SWIR is set to 0 before enabling the interrupt after a reset.

3000 and 4000 Series CPU Interrupt Registers

This section describes the registers used to interrupt the CPU in 3000 and 4000 series systems.

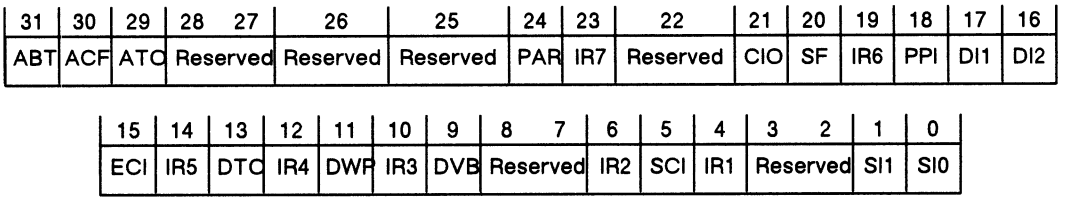
IEN0, IEN1 (3000 and 4000 Series Only) Interrupt Enable

IEN0 **Address FFF8 4004** **Write**

IEN1 **Address FFF8 4008** **Write**

The Interrupt Enable registers (IEN0 and IEN1) enable and mask interrupts to the CPUs. IEN0 and IEN1 enable interrupts to CPU0 and CPU1, respectively (a single-processor system uses only IEN0). To enable an interrupt, write a 1 into the corresponding bit in IEN0 or IEN1. To mask an interrupt, write a 0 into the corresponding bit in IEN0 or IEN1. The bits in the IST register and the Interrupt Enable registers are mirror images of each other. A system reset clears all Interrupt Enable register bits to 0; a local reset does not affect these registers.

The following bitbox and bit descriptions delete the Z-buffer (ZBF), Video (VDI), and keyboard (KBD) interrupts.



Bit	Name	Function
31	ABT	Abort. 1 Enables the abort pushbutton interrupt. 0 Masks the abort pushbutton interrupt.
30	ACF	Ac failure. 1 Enables the ac power failure interrupt. 0 Masks the ac power failure interrupt.
29	ATO	VMEbus timeout. 1 Enables the VMEbus timeout interrupt. 0 Masks the VMEbus timeout interrupt.
28, 27	Reserved	Write a 0 to these bits.
26	Reserved	Was Zbuffer interrupt
25	Reserved	Was Video interrupt

(continued)

Bit	Name	Function
24	PAR	Parity error. 1 Enables the parity error interrupt. 0 Masks the parity error interrupt.
23	IR7	VMEbus level 7. 1 Enables the level 7 interrupt from the VMEbus. 0 Masks the level 7 interrupt from the VMEbus.
22	Reserved	Was Keyboard interrupt
21	CIO	CIO. 1 Enables the CIO interrupt. 0 Masks the CIO interrupt.
20	SF	System failure. 1 Enables the system failure interrupt. 0 Masks the system power failure interrupt.
19	IR6	VMEbus level 6. 1 Enables the level 6 interrupt from the VMEbus. 0 Masks the level 6 interrupt from the VMEbus.
18	PPI	Parallel port. 1 Enables the parallel port request interrupt. 0 Masks the parallel port request interrupt.
17	DI1	DUART1. 1 Enables the DUART1 interrupt. 0 Masks the DUART1 interrupt.
16	DI2	DUART2. 1 Enables the DUART2 interrupt. 0 Masks the DUART2 interrupt.
15	ECI	Ethernet controller. 1 Enables the Ethernet controller request interrupt. 0 Masks the Ethernet controller request interrupt.
14	IR5	VMEbus level 5. 1 Enables the level 5 interrupt from the VMEbus. 0 Masks the level 5 interrupt from the VMEbus.
13	DTC	DMA terminal count 1 Enables the DMA terminal count interrupt. 0 Masks the DMA terminal count interrupt.
12	IR4	VMEbus level 4. 1 Enables the level 4 interrupt from the VMEbus. 0 Masks the level 4 interrupt from the VMEbus.
11	DWP	DMA write protect error. 1 Enables the DMA write protect error interrupt. 0 Masks the DMA write protect error interrupt.
10	IR3	VMEbus level 3. 1 Enables the level 3 interrupt from the VMEbus. 0 Masks the level 3 interrupt from the VMEbus.

(continued)

Bit	Name	Function
9	DVB	DMA valid bit. 1 Enables the DMA valid bit interrupt. 0 Masks the DMA valid bit interrupt.
8, 7	Reserved	Write a 0 to these bits.
6	IR2	VMEbus level 2. 1 Enables the level 2 interrupt from the VMEbus. 0 Masks the level 2 interrupt from the VMEbus.
5	SCI	SCSI controller. 1 Enables the SCSI controller request interrupt. 0 Masks the SCSI controller request interrupt.
4	IR1	VMEbus level 1. 1 Enables the level 1 interrupt from the VMEbus. 0 Masks the level 1 interrupt from the VMEbus.
3, 2	Reserved	Write a 0 to these bits.
1	SI1	Software-generated interrupt 1. 1 Enables software interrupt 1. 0 Masks software interrupt 1.
0	SI0	Software-generated interrupt 0. 1 Enables software interrupt 0. 0 Masks software interrupt 0.

(concluded)

IST (3000 and 4000 Series Only) — Interrupt Status

Address FFF8 4040 — Read

The Interrupt Status (IST) register contains the current state of all interrupt requests. When a device generates an interrupt, the interrupt logic sets the corresponding bit in the IST register.

To service an interrupt, the interrupt service routine reads the IST register, and possibly one of the Interrupt Enable registers (IEN, IEN0 or IEN1) to determine whether or not the interrupt is masked. The interrupt service routine services the highest-priority interrupt. The bits in the Interrupt Enable registers and the Interrupt Status register are mirror images of each other.

Resets do not affect IST bits; IST can only be cleared by software.

The following bitbox and bit descriptions delete the Z-buffer (ZBF), Video (VDI), and keyboard (KBD) interrupts.

31	30	29	28 27	26	25	24	23	22	21	20	19	18	17	16
ABT	ACF	ATO	Reserved	Reserved	Reserved	PAR	IR7	Reserved	CIO	SF	IR6	PPI	DI1	DI2

15	14	13	12	11	10	9	8 7	6	5	4	3 2	1	0
ECI	IR5	DTO	IR4	DWP	IR3	DVB	Reserved	IR2	SCI	IR1	Reserved	SI1	SI0

Bit	Name	Function
31	ABT	Abort pushbutton. 1 The abort pushbutton has been depressed since the last write to the CAB bit in the CLRINT register. 0 The abort pushbutton has not been depressed since the last write to the CAB bit in the CLRINT register.
30	ACF	Ac failure. 1 An ac power failure has occurred since the last write to the ACF bit in the CLRINT register. The ac failure signal originates from the power supply, which is connected to the VMEbus. 0 No ac power failure has occurred.
29	ATO	VMEbus arbitration timeout. 1 The VMEbus bus grant has timed out and generated an interrupt. 0 No VMEbus timeout has occurred.
28, 27	Reserved	Reserved and read as 0.
26	Reserved	Was Zbuffer interrupt
25	Reserved	Was Video interrupt

(continued)

Bit	Name	Function
24	PAR	Parity error. 1 A parity error has occurred. 0 No parity error has occurred.
23	IR7	VME level 7. 1 A VMEbus level 7 interrupt has occurred. 0 No VMEbus level 7 interrupt has occurred.
22	Reserved	Was Keyboard interrupt
21	CIO	CIO. 1 The CIO is requesting an interrupt. 0 The CIO is not requesting an interrupt.
20	SF	System failure. 1 A system failure signal has occurred since the last write to the CSF bit in the CLRINT register. This is the SYSFAIL* signal on the VMEbus and not a workstation failure. 0 No system failure has occurred.
19	IR6	VME level 6. 1 A VME level 6 interrupt has occurred. 0 No VME level 6 interrupt has occurred.
18	PPI	Parallel port. 1 The parallel port is requesting an interrupt. 0 The parallel port is not requesting an interrupt.
17	DI1	DUART1. 1 DUART1 is requesting an interrupt. 0 DUART1 is not requesting an interrupt.
16	DI2	DUART2. 1 DUART2 is requesting an interrupt. 0 DUART2 is not requesting an interrupt.
15	ECI	Ethernet controller. 1 The Ethernet controller is requesting an interrupt. 0 The Ethernet controller is not requesting an interrupt.
14	IR5	VMEbus level 5. 1 A VMEbus level 5 interrupt has occurred. 0 A VMEbus level 5 interrupt has not occurred.
13	DTC	DMA terminal count 1 The DMA terminal count has been reached. 0 The DMA terminal count has not been reached.
12	IR4	VMEbus level 4. 1 A VMEbus level 4 interrupt has occurred. 0 No VMEbus level 4 interrupt has occurred.
11	DWP	DMA write protect error. 1 A DMA write protect error has occurred. 0 No DMA write protect error has occurred.
10	IR3	VMEbus level 3. 1 A VMEbus level 3 interrupt has occurred. 0 No VMEbus level 3 interrupt has occurred.

(continued)

Chapter 7
Programming the Serial Ports and Parallel Port

This chapter describes the following topics:

- The serial and parallel ports.
- Serial port registers and how to program the serial ports.
- Parallel port registers and how to program the parallel ports.

Overview of the Serial and Parallel Ports

AViiON 3000 and 4000 series systems have two RS-232-C asynchronous serial ports that support modems. These systems do not support RS-422.

Both the 3000 and 4000 series systems have a parallel port that supports either a Data Products interface or a Centronics interface.

The I/O signals are described in Appendix D, "System Board Connectors."

Components of the Serial and Parallel Ports

3000 and 4000 series stations have two DUARTs (DUART1 and DUART2) that control two serial ports and a parallel port. The figure below replaces Figure 7–1.

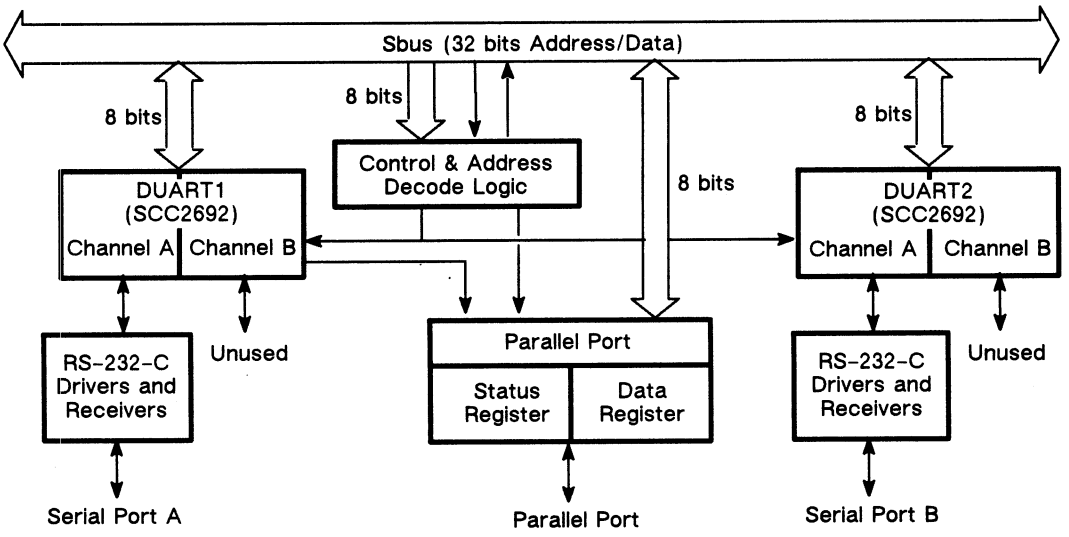


Figure 7–1 3000 and 4000 Series Serial and Parallel Ports

Appendix D
System Board Connectors

This appendix identifies the connectors and signals available on your workstation. Table D–1 lists the connectors for the workstations. Figure D–1 identifies the external connectors on 3000 series stations, and Figure D–2 identifies the system board connectors on 3000 series stations. Figure D–3 identifies the external connectors on 4000 series stations, and Figure D–4 identifies the system board connectors on 4000 series stations. The remainder of the Appendix describes the signals present in the connectors.

Table D–1 Connectors on the System Board

Subsystem	Connector Number	Connector Type
LAN interface	J6	D15 (Female)
Serial port (300 Series)	J10	D25 (Male)
Serial ports (400 Series)	J4, J10	D25 (Male)
Parallel port	J7	D25 (Female)
SCSI port	J5	D50
VMEbus (400 Series)	J30, J31	96-pin

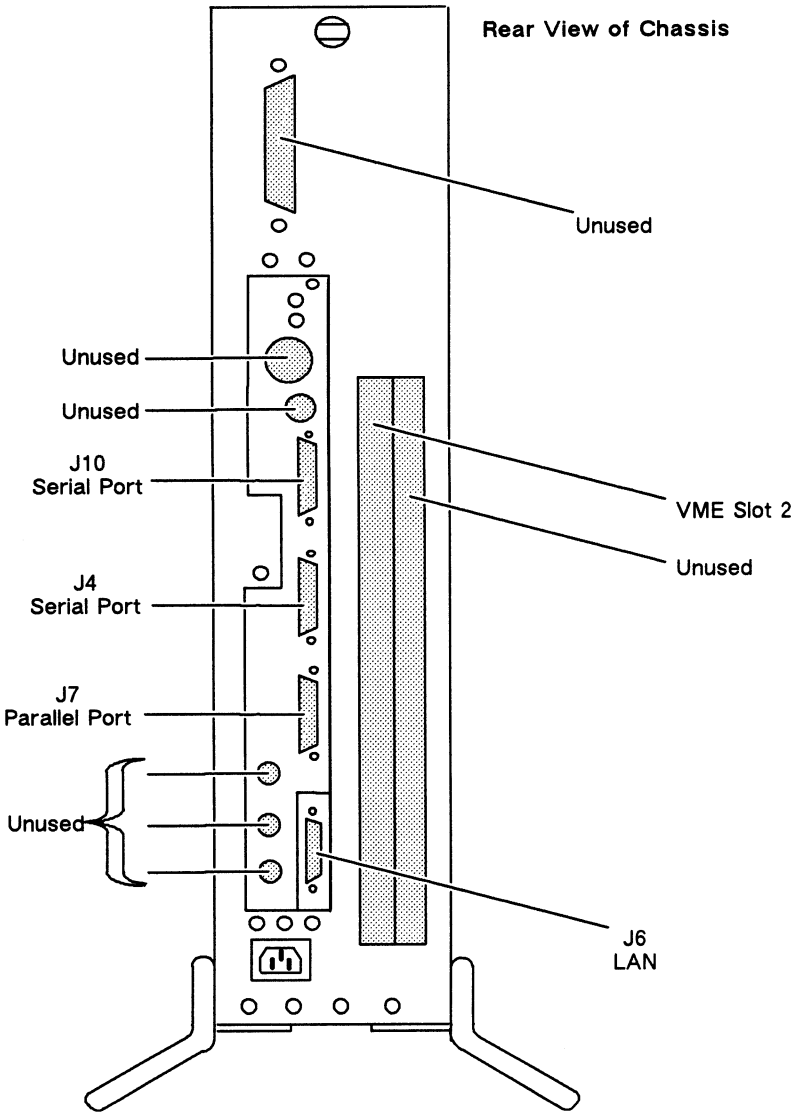
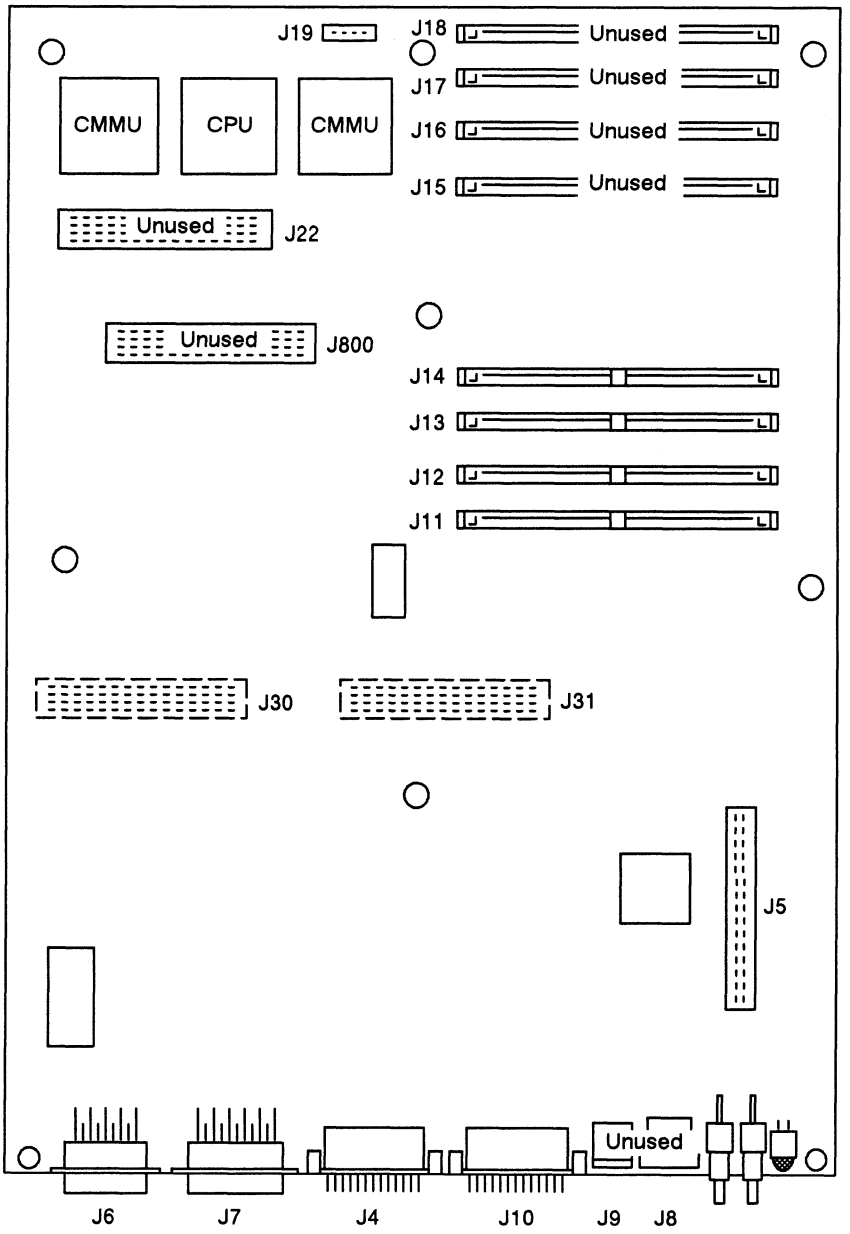


Figure D–1 3000 Series External Connectors



J4	Serial Port #1	J11	Memory Board 1
J5	SCSI Bus	J12	Memory Board 2
J6	Ethernet LAN	J13	Memory Board 3
J7	Parallel Port	J14	Memory Board 4
J8	Unused	J15	Unused
J9	Unused	J16	Unused
J10	Serial Port #2	J17	Unused
J19	Speaker and LED	J18	Unused
J22	Unused		
J30	VMEbus (P1)		
J31	VMEbus (P2)		
J800	Unused		

Figure D–2 3000 Series System Board Connectors

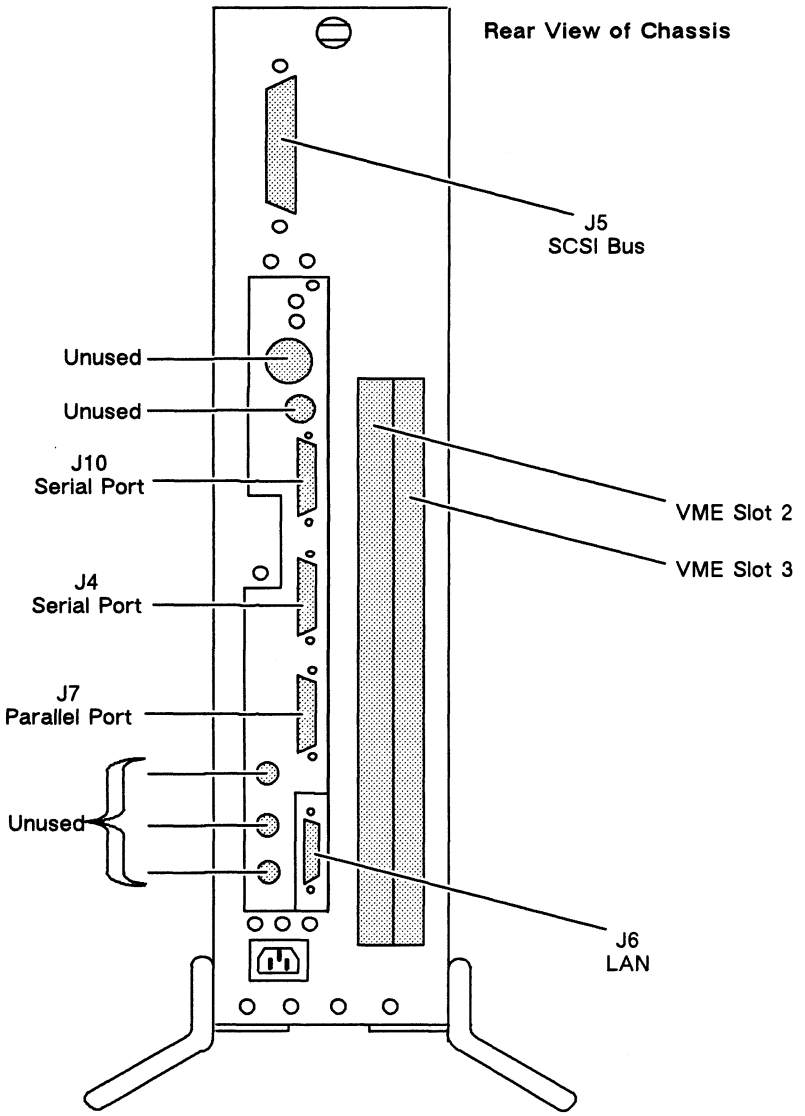
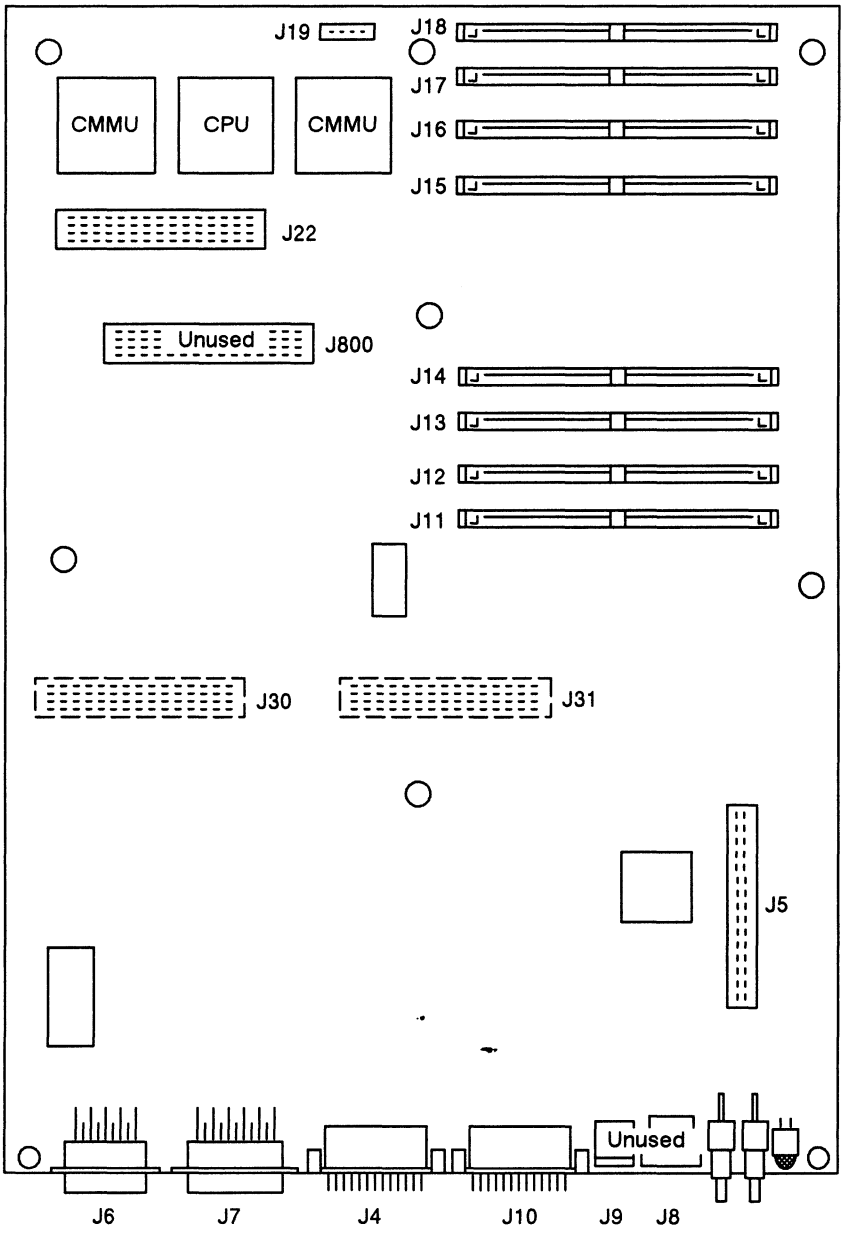


Figure D–3 4000 Series External Connectors



J4	Serial Port #1	J11	Memory Board 1
J5	SCSI Bus	J12	Memory Board 2
J6	Ethernet LAN	J13	Memory Board 3
J7	Parallel Port	J14	Memory Board 4
J8	Unused	J15	Memory Board 5
J9	Unused	J16	Memory Board 6
J10	Serial Port #2	J17	Memory Board 7
J19	Speaker and LED	J18	Memory Board 8
J22	Optional CPU Set (Mezzanine Board)		
J30	VMEbus (P1)		
J31	VMEbus (P2)		
J800	Unused		

Figure D–4 4000 Series System Board Connectors

Serial Port Connector (300 Series)

Serial devices connect to the serial port through a 25-pin D-connector (J10). Table D-2 identifies the serial port signals.

Table D-2 Serial Connector Signals (300 Series)

Pin	Signal	Direction
1	CG (RS-232-C)	-----
2	TxD (RS-232-C)	From system board
3	RxD (RS-232-C)	To system board
4	RTS (RS-232-C)	From system board
5	CTS (RS-232-C)	To system board
6	DSR (RS-232-C)	To system board
7	SG (RS-232-C)	-----
8	DCD (RS-232-C)	To system board
9	RxD + (RS-422)	To system board
10	RxD - (RS-422)	To system board
11	TxD + (RS-422)	From system board
12	TxD - (RS-422)	From system board
13	RS-422 Select (Ground selects RS-422)	To system board
14-19	Unused	-----
20	DTR (RS-232-C)	From system board
21	Unused	-----
22	RI (RS-232-C)	To system board
23-25	Unused	-----

Serial Port Connectors (400 Series)

Serial devices connect to the serial port through 25-pin D-connectors (J4 and J10). J4 is channel A and J10 is channel B. Table D-3 identifies the serial port signals.

Table D-3 Serial Connector Signals (400 Series)

Pin	Signal	Direction
1	CG	-----
2	TxD	From system board
3	RxD	To system board
4	RTS	From system board
5	CTS	To system board
6	DSR	To system board
7	SG	-----
8	DCD	To system board
9-19	Unused	-----
20	DTR	From system board
21	Unused	-----
22	RI	To system board
23-25	Unused	-----

LAN Connector

The LAN interface provides a D15 connector for an AUI cable. The AUI cable connects the workstation to an external medium attachment unit (MAU). The MAU contains the Ethernet transceiver and the medium dependent interface (MDI) for connection to the physical network. The MAU provides electrical isolation between the AUI cable and the physical network. The Ethernet interface can be attached via the AUI cable to any one of the following types of external 10-MHz MAUs: 10BASE5 (Ethernet), 10BASE2 (Cheapernet or Thin Ethernet), 10BROAD36 (Ethernet over CATV), 10BASET (proposed Ethernet over twisted pair), or any other 10-MHz AUI compatible MAU or MAU-like device that does not require the Control Out signal specified in the AUI definition. Table D-12 identifies the LAN signals.

Table D-12 LAN Interface Connector Signals

Pin	Signal	Circuit Name
1	Ground	CI-S (Control In Shield)
2	Collision +	CI-A (Control In A)
3	Transmit +	DO-A (Data Out A)
4	Ground	DI-S (Data In Shield)
5	Receive +	DI-A (Data In A)
6	Ground	VC (Voltage Common)
7	No Connection	CO-A (Control Out circuit A)
8	Ground	CO-S (Control Out Shield)
9	Collision -	CI-B (Control In B)
10	Transmit -	DO-B (Data Out B)
11	Ground	DO-S (Data Out Shield)
12	Receive -	DI-B (Data In B)
13	+12 V	VP (Voltage Plus)
14	Ground	VS (Voltage Shield)
15	No Connection	CO-B (Control Out B)
Shell	Ground	PG (Protective Ground)

VMEbus Connectors (3000 Series)

Figure D–5 shows the location of the VMEbus slots and connectors and identifies the pin and row positions. Table D–13 identifies the VMEbus signals on connector J1; Table D–14 identifies the VMEbus signals on connector J2. The manual *The VMEbus Specification* describes the signals and interface in detail.

The figure below replaces Figure D–5 for 3000 series systems.

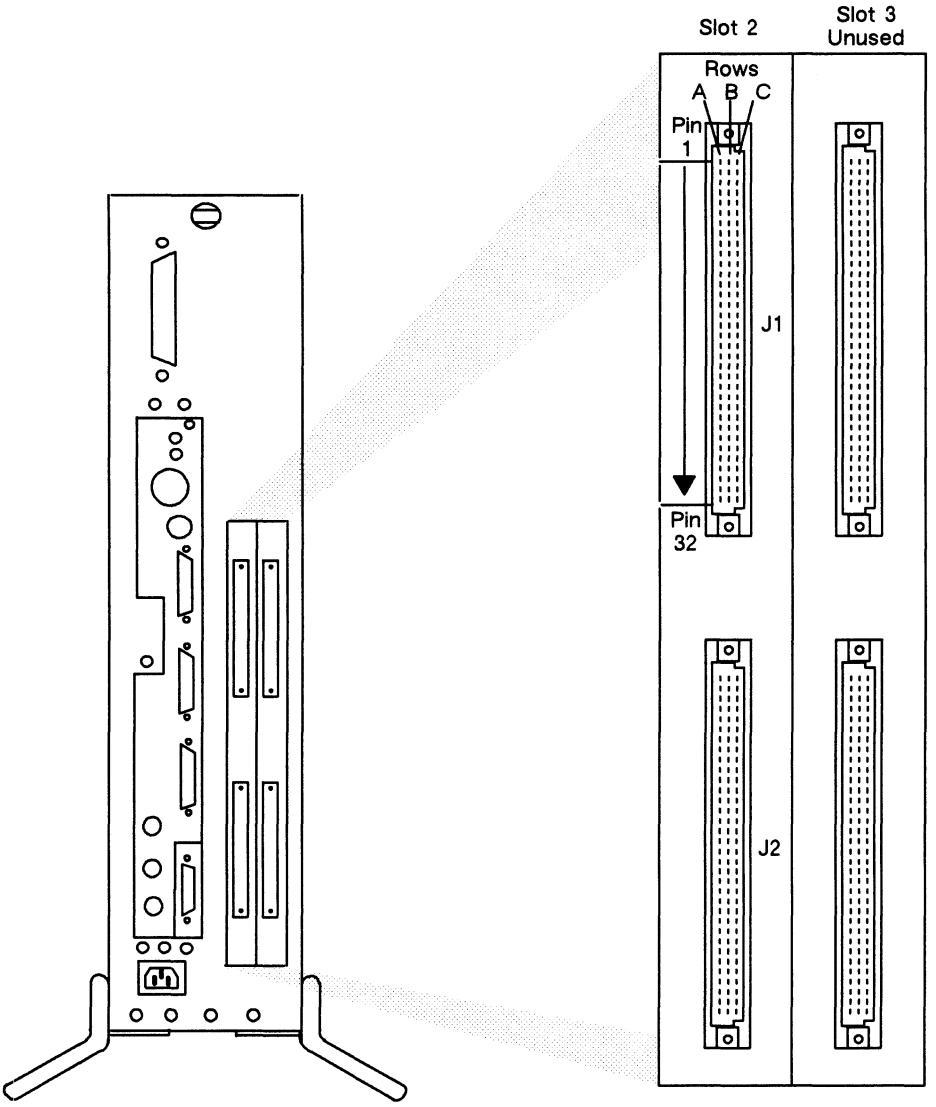


Figure D–5 3000 Series VMEbus Connectors

TIPS ORDERING PROCEDURES

TO ORDER

1. An order can be placed with the TIPS group in two ways:
   a) MAIL ORDER – Use the order form on the opposite page and fill in all requested information. Be sure to include shipping charges and local sales tax. If applicable, write in your tax exempt number in the space provided on the order form.

      Send your order form with payment to:

      Data General Corporation
      ATTN: Educational Services/TIPS G155
      4400 Computer Drive
      Westboro, MA 01581-9973

   b) TELEPHONE – Call TIPS at (508) 870-1600 for all orders that will be charged by credit card or paid for by purchase orders over $50.00. Operators are available from 8:30 AM to 5:00 PM EST.

METHOD OF PAYMENT

2. As a customer, you have several payment options:
   a) Purchase Order – Minimum of $50. If ordering by mail, a hard copy of the purchase order must accompany order.
   b) Check or Money Order – Make payable to Data General Corporation.
   c) Credit Card – A minimum order of $20 is required for Mastercard or Visa orders.

SHIPPING

3. To determine the charge for UPS shipping and handling, check the total quantity of units in your order and refer to the following chart:

Total Quantity	Shipping & Handling Charge
1-4 Units	$5.00
5-10 Units	$8.00
11-40 Units	$10.00
41-200 Units	$30.00
Over 200 Units	$100.00

   If overnight or second day shipment is desired, this information should be indicated on the order form. A separate charge will be determined at time of shipment and added to your bill.

VOLUME DISCOUNTS

4. The TIPS discount schedule is based upon the total value of the order.

Order Amount	Discount
$1-$149.99	0%
$150-$499.99	10%
Over $500	20%

TERMS AND CONDITIONS

5. Read the TIPS terms and conditions on the reverse side of the order form carefully. These must be adhered to at all times.

DELIVERY

6. Allow at least two weeks for delivery.

RETURNS

7. Items ordered through the TIPS catalog may not be returned for credit.
8. Order discrepancies must be reported within 15 days of shipment date. Contact your TIPS Administrator at (508) 870-1600 to notify the TIPS department of any problems.

INTERNATIONAL ORDERS

9. Customers outside of the United States must obtain documentation from their local Data General Subsidiary or Representative. Any TIPS orders received by Data General U.S. Headquarters will be forwarded to the appropriate DG Subsidiary or Representative for processing.

TIPS ORDER FORM

Mail To: Data General Corporation
Attn: Educational Services/TIPS G155
4400 Computer Drive
Westboro, MA 01581 - 9973

BILL TO:	SHIP TO: (No P.O. Boxes - Complete Only If Different Address)
COMPANY NAME	COMPANY NAME
ATTN:	ATTN:
ADDRESS	ADDRESS (NO PO BOXES)
CITY	CITY
STATE ZIP	STATE ZIP

Priority Code _____ (See label on back of catalog)

Authorized Signature of Buyer (Agrees to terms & conditions on reverse side) | Title | Date | Phone (Area Code) | Ext.

ORDER #	QTY	DESCRIPTION	UNIT PRICE	TOTAL PRICE

A SHIPPING & HANDLING

☐ UPS	ADD
1-4 Items	$ 5.00
5-10 Items	$ 8.00
11-40 Items	$ 10.00
41-200 Items	$ 30.00
200+ Items	$100.00

Check for faster delivery

Additional charge to be determined at time of shipment and added to your bill.

☐ UPS Blue Label (2 day shipping)
☐ Red Label (overnight shipping)

B VOLUME DISCOUNTS

Order Amount	Save
$0 - $149.99	0%
$150 - $499.99	10%
Over $500.00	20%

Tax Exempt # or Sales Tax (if applicable) _____

ORDER TOTAL	
Less Discount See B	-
SUB TOTAL	
Your local* sales tax	+
Shipping and handling - See A	+
TOTAL - See C	

C PAYMENT METHOD

☐ Purchase Order Attached ($50 minimum)
P.O. number is_____. (Include hardcopy P.O.)
☐ Check or Money Order Enclosed
☐ Visa ☐ MasterCard ($20 minimum on credit cards)

Account Number ☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐☐ Expiration Date ☐☐☐☐

_____
Authorized Signature
(Credit card orders without signature and expiration date cannot be processed.)

THANK YOU FOR YOUR ORDER

PRICES SUBJECT TO CHANGE WITHOUT PRIOR NOTICE.
PLEASE ALLOW 2 WEEKS FOR DELIVERY.
NO REFUNDS NO RETURNS.

* Data General is required by law to collect applicable sales or use tax on all purchases shipped to states where DG maintains a place of business, which covers all 50 states. Please include your local taxes when determining the total value of your order. If you are uncertain about the correct tax amount, please call 508-870-1600.

Form 702
Rev. 8/87

DATA GENERAL CORPORATION
TECHNICAL INFORMATION AND PUBLICATIONS SERVICE
TERMS AND CONDITIONS

Data General Corporation ("DGC") provides its Technical Information and Publications Service (TIPS) solely in accordance with the following terms and conditions and more specifically to the Customer signing the Educational Services TIPS Order Form. These terms and conditions apply to all orders, telephone, telex, or mail. By accepting these products the Customer accepts and agrees to be bound by these terms and conditions.

1. CUSTOMER CERTIFICATION
Customer hereby certifies that it is the owner or lessee of the DGC equipment and/or licensee/sub-licensee of the software which is the subject matter of the publication(s) ordered hereunder.

2. TAXES
Customer shall be responsible for all taxes, including taxes paid or payable by DGC for products or services supplied under this Agreement, exclusive of taxes based on DGC's net income, unless Customer provides written proof of exemption.

3. DATA AND PROPRIETARY RIGHTS
Portions of the publications and materials supplied under this Agreement are proprietary and will be so marked. Customer shall abide by such markings. DGC retains for itself exclusively all proprietary rights (including manufacturing rights) in and to all designs, engineering details and other data pertaining to the products described in such publication. Licensed software materials are provided pursuant to the terms and conditions of the Program License Agreement (PLA) between the Customer and DGC and such PLA is made a part of and incorporated into this Agreement by reference. A copyright notice on any data by itself does not constitute or evidence a publication or public disclosure.

4. LIMITED MEDIA WARRANTY
DGC warrants the CLI Macros media, provided by DGC to the Customer under this Agreement, against physical defects for a period of ninety (90) days from the date of shipment by DGC. DGC will replace defective media at no charge to you, provided it is returned postage prepaid to DGC within the ninety (90) day warranty period. This shall be your exclusive remedy and DGC's sole obligation and liability for defective media. This limited media warranty does not apply if the media has been damaged by accident, abuse or misuse.

5. DISCLAIMER OF WARRANTY
EXCEPT FOR THE LIMITED MEDIA WARRANTY NOTED ABOVE, DGC MAKES NO WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE ON ANY OF THE PUBLICATIONS, CLI MACROS OR MATERIALS SUPPLIED HEREUNDER.

6. LIMITATION OF LIABILITY
A. CUSTOMER AGREES THAT DGC'S LIABILITY, IF ANY, FOR DAMAGES, INCLUDING BUT NOT LIMITED TO LIABILITY ARISING OUT OF CONTRACT, NEGLIGENCE, STRICT LIABILITY IN TORT OR WARRANTY SHALL NOT EXCEED THE CHARGES PAID BY CUSTOMER FOR THE PARTICULAR PUBLICATION OR CLI MACRO INVOLVED. THIS LIMITATION OF LIABILITY SHALL NOT APPLY TO CLAIMS FOR PERSONAL INJURY CAUSED SOLELY BY DGC'S NEGLIGENCE. OTHER THAN THE CHARGES REFERENCED HEREIN, IN NO EVENT SHALL DGC BE LIABLE FOR ANY INCIDENTAL, INDIRECT, SPECIAL OR CONSEQUENTIAL DAMAGES WHATSOEVER, INCLUDING BUT NOT LIMITED TO LOST PROFITS AND DAMAGES RESULTING FROM LOSS OF USE, OR LOST DATA, OR DELIVERY DELAYS, EVEN IF DGC HAS BEEN ADVISED, KNEW OR SHOULD HAVE KNOWN OF THE POSSIBILITY THEREOF; OR FOR ANY CLAIM BY ANY THIRD PARTY.

B. ANY ACTION AGAINST DGC MUST BE COMMENCED WITHIN ONE (1) YEAR AFTER THE CAUSE OF ACTION ACCRUES.

7. GENERAL
A valid contract binding upon DGC will come into being only at the time of DGC's acceptance of the referenced Educational Services Order Form. Such contract is governed by the laws of the Commonwealth of Massachusetts, excluding its conflict of law rules. Such contract is not assignable. These terms and conditions constitute the entire agreement between the parties with respect to the subject matter hereof and supersedes all prior oral or written communications, agreements and understandings. These terms and conditions shall prevail notwithstanding any different, conflicting or additional terms and conditions which may appear on any order submitted by Customer. DGC hereby rejects all such different, conflicting, or additional terms.

8. IMPORTANT NOTICE REGARDING AOS/VS INTERNALS SERIES (ORDER #1865 & #1875)
Customer understands that information and material presented in the AOS/VS Internals Series documents may be specific to a particular revision of the product. Consequently user programs or systems based on this information and material may be revision-locked and may not function properly with prior or future revisions of the product. Therefore, Data General makes no representations as to the utility of this information and material beyond the current revision level which is the subject of the manual. Any use thereof by you or your company is at your own risk. Data General disclaims any liability arising from any such use and I and my company (Customer) hold Data General completely harmless therefrom.

134-755-02

moisten & seal

CUSTOMER DOCUMENTATION COMMENT FORM

Your Name _____ Your Title _____

Company _____ Phone _____

Street _____

City _____ State _____ Zip _____

We wrote this book for you, and we made certain assumptions about who you are and how you would use it. Your comments will help us correct our assumptions and improve the manual. Please take a few minutes to respond. Thank you.

Manual Title _____ Manual No. _____

Who are you?
☐EDP/MIS Manager ☐Analyst/Programmer ☐Other _____
☐Senior Systems Analyst ☐Operator _____
☐Engineer ☐End User

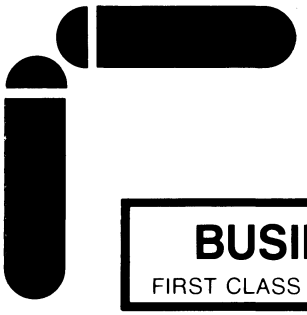
How do you use this manual? *(List in order: 1 = Primary Use)*

___ Introduction to the product ___ Tutorial Text ___ Other
___ Reference ___ Operating Guide _____

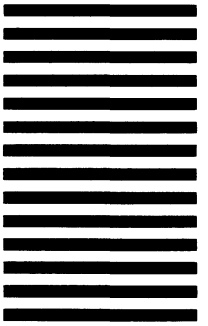
		Yes	No
About the manual:	Is it easy to read?	☐	☐
	Is it easy to understand?	☐	☐
	Are the topics logically organized?	☐	☐
	Is the technical information accurate?	☐	☐
	Can you easily find what you want?	☐	☐
	Does it tell you everything you need to know?	☐	☐
	Do the illustrations help you?	☐	☐

If you wish to order manuals, use the enclosed TIPS Order Form (USA only) or contact your sales representative or dealer.

Comments:



NO POSTAGE
NECESSARY
IF MAILED
IN THE
UNITED STATES



BUSINESS REPLY MAIL

FIRST CLASS PERMIT NO. 26 WESTBORO, MA 01581

POSTAGE WILL BE PAID BY ADDRESSEE

DataGeneral

Customer Documentation
MS E-111
4400 Computer Drive
P.O. Box 4400
Westboro, MA 01581-9890

134-755-02

Technical Notice for AViiON™ 3000 and 4000 Series Systems: Programming System Control and I/O Registers

014-001878-00

Cut here and insert in binder spine pocket

DataGeneral
Data General Corporation, Westboro, Massachusetts 01580

014-001878-00